Synchronous DRAM

MT48LC128M4A2 – 32 Meg x 4 x 4 banks
MT48LC64M8A2 – 16 Meg x 8 x 4 banks
MT48LC32M16A2 – 8 Meg x 16 x 4 banks

For the latest data sheet, refer to Micron's Web site

Features

- PC100- and PC133-compliant
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto precharge, includes concurrent auto precharge, and auto refresh modes
- Self refresh mode
- 64ms, 8,192-cycle refresh
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply

Table 1: Address Table

Parameter	32 Meg x 4	32 Meg x 8	32 Meg x 16
Configuration	32 Meg x 4 x 4 banks	16 Meg x 8 x 4 banks	8 Meg x 16 x 4 banks
Refresh count	8K	8K	8K
Row addressing	8K (A0–A12)	8K (A0–A12)	8K (A0–A12)
Bank addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column addressing	4K (A0–A9, A11, A12)	2K (A0–A9, A11)	1K (A0–A9)

Table 2: Key Timing Parameters

Speed Grade	Clock Frequency	Access Time		Setup Time	Hold Time
		CL = 2	CL = 3		
-7E	143 MHz	–	5.4ns	1.5ns	0.8ns
-75	133 MHz	–	5.4ns	1.5ns	0.8ns
-7E	133 MHz	5.4ns	–	1.5ns	0.8ns
-75	100 MHz	6ns	–	1.5ns	0.8ns

Part Number Example:
MT48LC32M16A2P-75:C

Options

Options	Marking
• Configurations	
– 128 Meg x 4 (32 Meg x 4 x 4 banks)	128M4
– 64 Meg x 8 (16 Meg x 8 x 4 banks)	64M8
– 32 Meg x 16 (8 Meg x 16 x 4 banks)	32M16
• WRITE recovery (^{t}WR)	
– ^{t}WR = "2 CLK"[1]	A2
• Plastic package – OCPL[2]	
– 54-pin TSOP II (400 mil)	TG
– 54-pin TSOP II (400 mil) Pb-free	P
• Timing (cycle time)	
– 7.5ns @ CL = 2 (PC133)	-7E[4]
– 7.5ns@ CL = 3 (PC133)	-75
• Self refresh	
– Standard	None
– Low power	L[3]
• Operating temperature range	
– Commercial (0°C to +70°C)	None
– Industrial (–40°C +85°C)	IT
• Revision	:C

Notes: 1. Refer to Micron technical note: TN-48-05.
2. Off-center parting line.
3. Contact factory for availability.
4. Available on x4 and x8 only.

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General Description

The 512Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x4's 134,217,728-bit banks is organized as 8,192 rows by 4,096 columns by 4 bits. Each of the x8's 134,217,728-bit banks is organized as 8,192 rows by 2,048 columns by 8 bits. Each of the x16's 134,217,728-bit banks is organized as 8,192 rows by 1,024 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A12 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths (BL) of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 512Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

The 512Mb SDRAM is designed to operate at 3.3V. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

Figure 1: 128 Meg x 4 SDRAM Functional Block Diagram

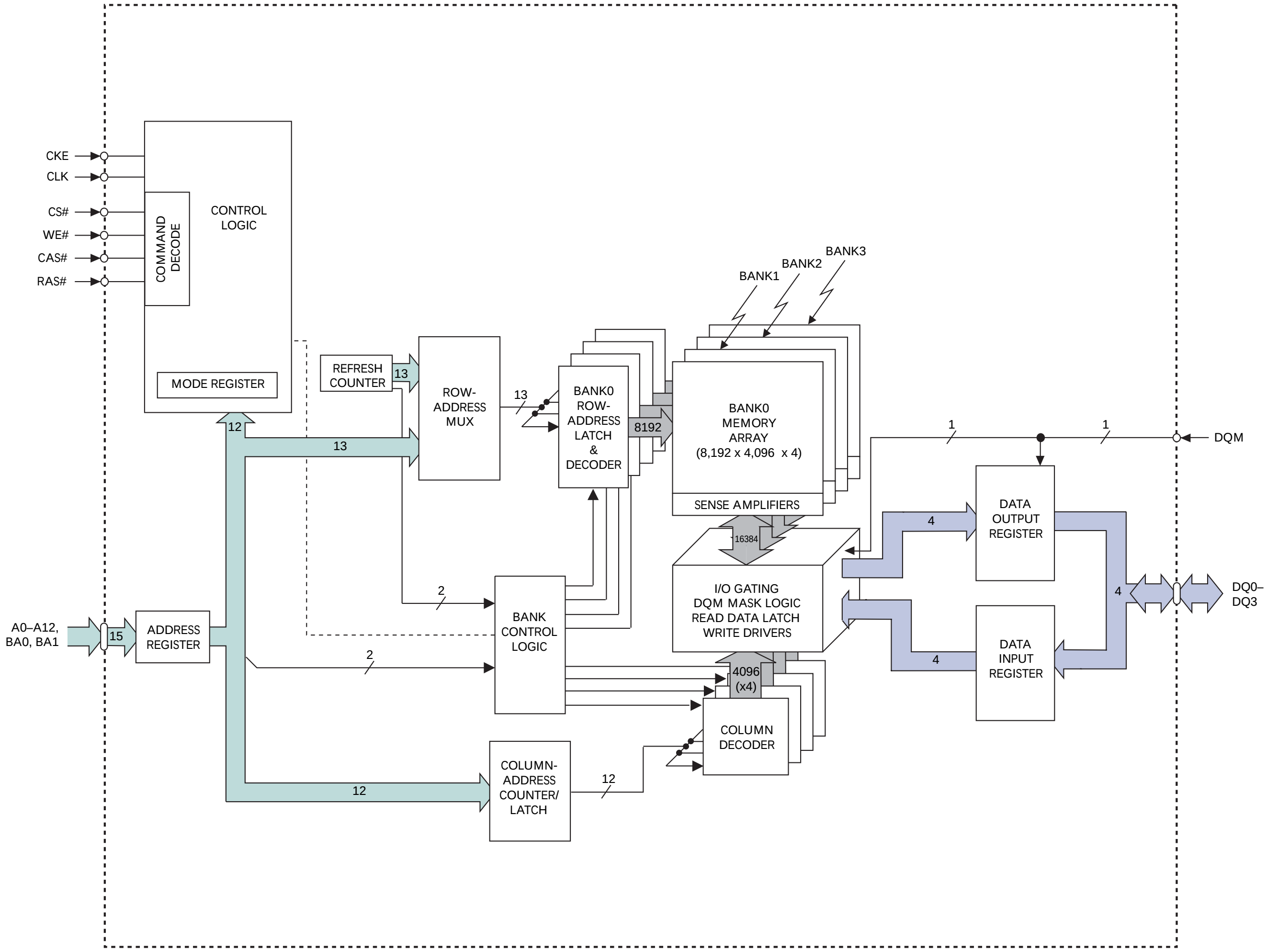


Figure 2: 64 Meg x 8 SDRAM Functional Block Diagram

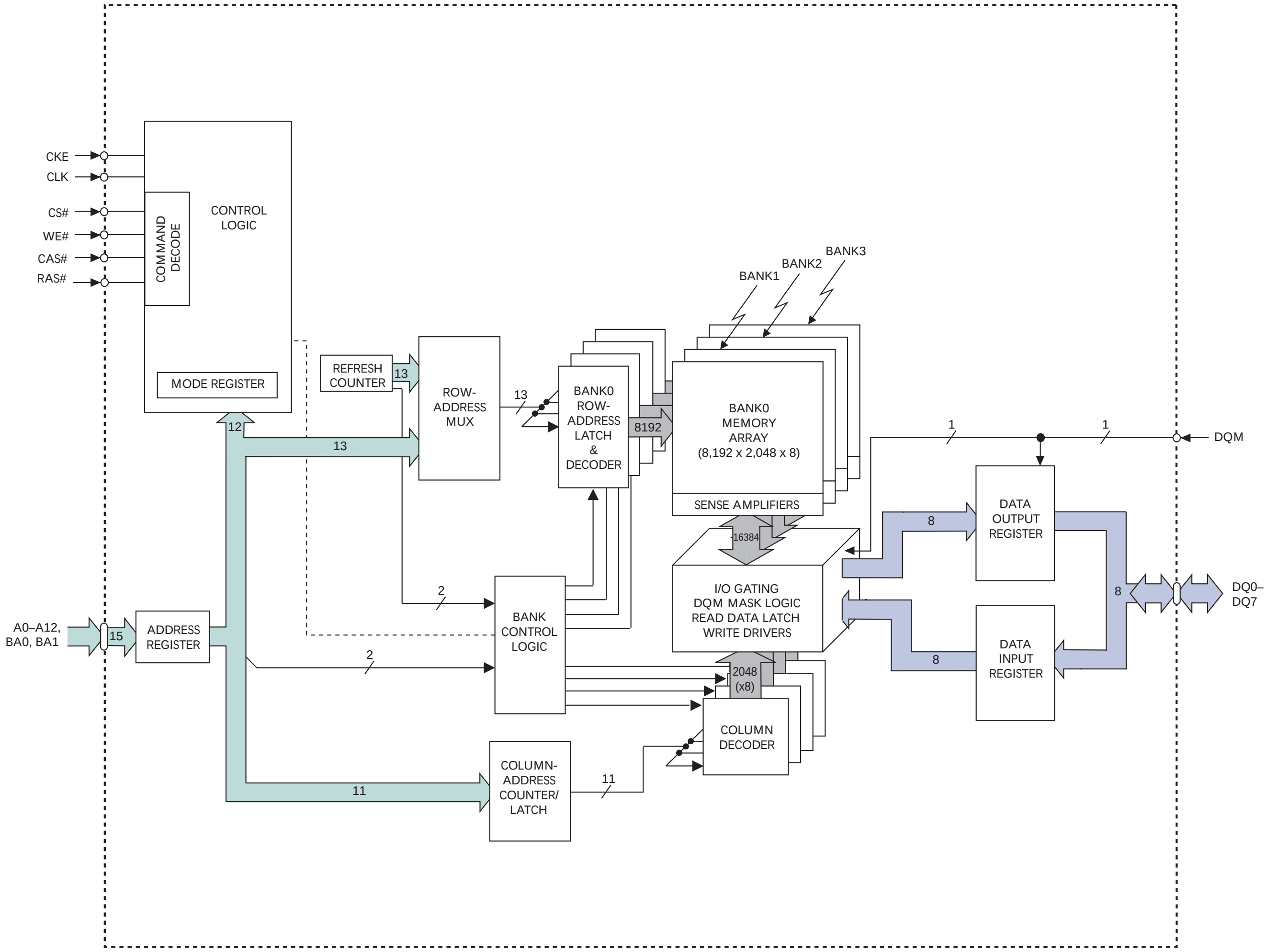


Figure 3: 32 Meg x 16 SDRAM Functional Block Diagram

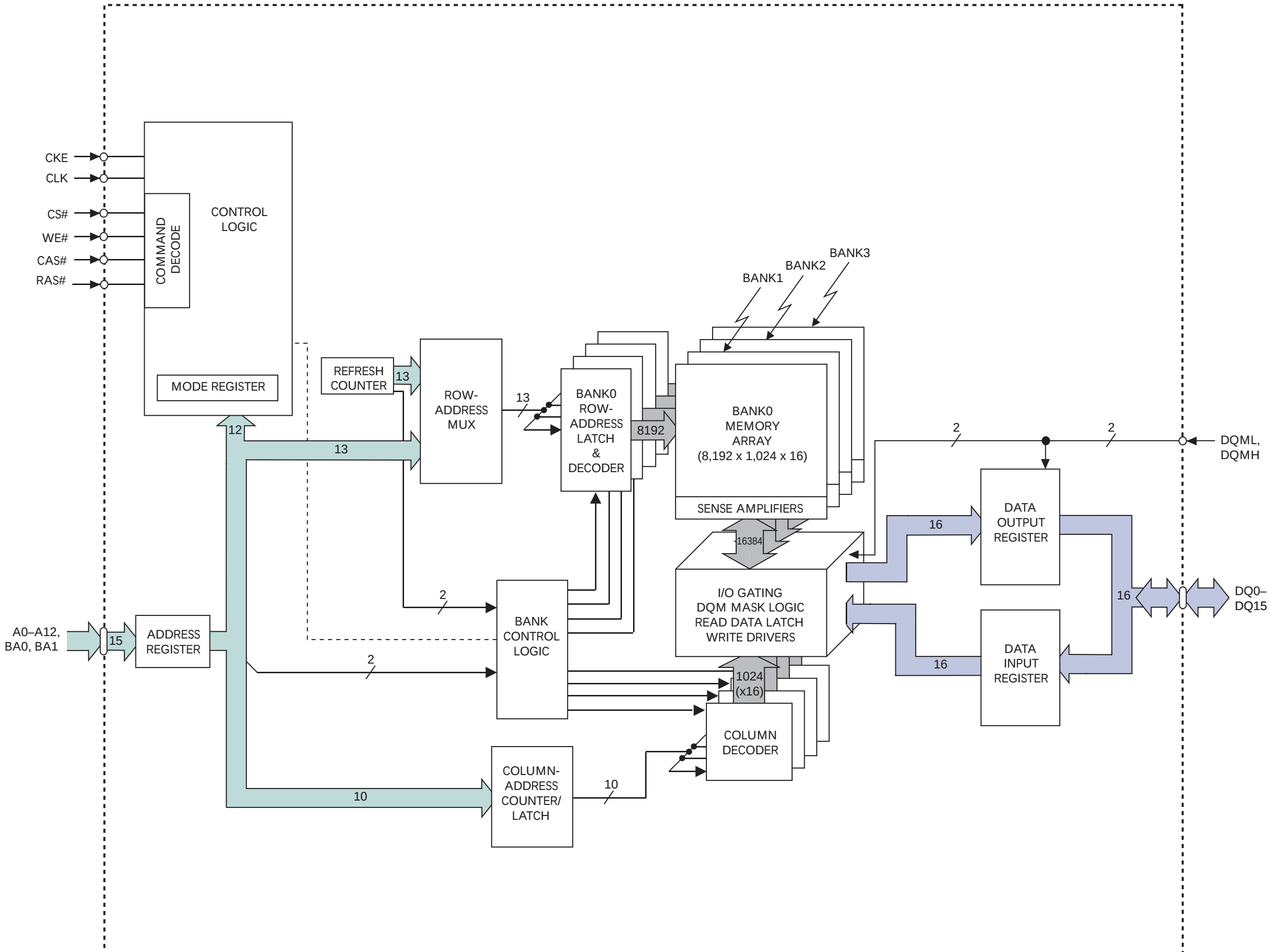


Figure 4: Pin Assignment (Top View) 54-Pin TSOP

x4	x8	x16	Pin	Pin	x16	x8	x4
-	-	VDD	1 •	54	VSS	-	-
NC	DQ0	DQ0	2	53	DQ15	DQ7	NC
-	-	VDDQ	3	52	VSSQ	-	-
NC	NC	DQ1	4	51	DQ14	NC	NC
DQ0	DQ1	DQ2	5	50	DQ13	DQ6	DQ3
-	-	VSSQ	6	49	VDDQ	-	-
NC	NC	DQ3	7	48	DQ12	NC	NC
NC	DQ2	DQ4	8	47	DQ11	DQ5	NC
-	-	VDDQ	9	46	VSSQ	-	-
NC	NC	DQ5	10	45	DQ10	NC	NC
DQ1	DQ3	DQ6	11	44	DQ9	DQ4	DQ2
-	-	VSSQ	12	43	VDDQ	-	-
NC	NC	DQ7	13	42	DQ8	NC	NC
-	-	VDD	14	41	VSS	-	-
NC	NC	DQML	15	40	NC	-	-
-	-	WE#	16	39	DQMH	DQM	DQM
-	-	CAS#	17	38	CLK	-	-
-	-	RAS#	18	37	CKE	-	-
-	-	CS#	19	36	A12	-	-
-	-	BA0	20	35	A11	-	-
-	-	BA1	21	34	A9	-	-
-	-	A10	22	33	A8	-	-
-	-	A0	23	32	A7	-	-
-	-	A1	24	31	A6	-	-
-	-	A2	25	30	A5	-	-
-	-	A3	26	29	A4	-	-
-	-	VDD	27	28	VSS	-	-

Note: The # symbol indicates signal is active LOW. A dash (-) indicates x8 and x4 pin function is same as x16 pin function.

Table 3: Pin Descriptions

Pin Numbers	Symbols	Type	Description
38	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
37	CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE power-down and SELF REFRESH operation (all banks idle), ACTIVE power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
19	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
18, 17, 16	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
39	x4, x8: DQM	Input	Input/output mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. On the x4 and x8, DQML (Pin 15) is a NC and DQMH is DQM. On the x16, DQML corresponds to DQ0–DQ7, and DQMH corresponds to DQ8–DQ15. DQML and DQMH are considered same state when referenced as DQM.
15, 39	x16: DQML, DQMH		
20, 21	BA0, BA1	Input	Bank address inputs: BA0 and BA1 define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
23–26, 29–34, 22, 35, 36	A0–A12	Input	Address inputs: A0–A12 are sampled during the ACTIVE command (row-address A0–A12) and READ/WRITE command (column-address A0–A9, A11, A12 [x4]; A0–A9, A11 [x8]; A0–A9 [x16]; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether all banks are to be precharged (A10 [HIGH]) or bank selected by (A10 [LOW]). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2, 4, 5, 7, 8, 10, 11, 13, 42, 44, 45, 47, 48, 50, 51, 53	DQ0–DQ15	x16: I/O	Data input/output: Data bus for x16 (4, 7, 10, 13, 15, 42, 45, 48, and 51 are NCs for x8; 2, 4, 7, 8, 10, 13, 15, 42, 45, 47, 48, 51, and 53 are NCs for x4).
2, 5, 8, 11, 44, 47, 50, 53	DQ0–DQ7	x8: I/O	Data input/output: Data bus for x8 (2, 8, 47, and 53 are NCs for x4).
5, 11, 44, 50	DQ0–DQ3	x4: I/O	Data input/output: Data bus for x4.
40	NC	–	No connect: This pin should be left unconnected.
3, 9, 43, 49	V_{DDQ}	Supply	DQ power: Isolated DQ power to the die for improved noise immunity.
6, 12, 46, 52	V_{SSQ}	Supply	DQ ground: Isolated DQ ground to the die for improved noise immunity.
1, 14, 27	V_{DD}	Supply	Power supply: +3.3V ±0.3V.
28, 41, 54	V_{SS}	Supply	Ground.

Functional Description

The 512Mb SDRAMs (32 Meg x 4 x 4 banks, 16 Meg x 8 x 4 banks, and 8 Meg x 16 x 4 banks) are quad-bank DRAMs that operate at 3.3V and include a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x4's 134,217,728-bit banks is organized as 8,192 rows by 4,096 columns by 4 bits. Each of the x8's 134,217,728-bit banks is organized as 8,192 rows by 2,048 columns by 8 bits. Each of the x16's 134,217,728-bit banks is organized as 8,192 rows by 1,024 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0–A12 select the row). The address bits (x4: A0–A9, A11, A12; x8: A0–A9, A11; x16: A0–A9) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. After power is applied to VDD and VDDQ (simultaneously) and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

After the 100µs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

If desired, the two AUTO REFRESH commands can be issued after the LMR command.

The recommended power-up sequence for SDRAMs:

1. Simultaneously apply power to VDD and VDDQ.
2. Assert and hold CKE at a LVTTL logic LOW since all inputs and outputs are LVTTL-compatible.
3. Provide stable CLOCK signal. Stable clock is defined as a signal cycling within timing constraints specified for the clock pin.
4. Wait at least 100µs prior to issuing any command other than a COMMAND INHIBIT or NOP.
5. Starting at some point during this 100µs period, bring CKE HIGH. Continuing at least through the end of this period, one or more COMMAND INHIBIT or NOP commands must be applied.
6. Perform a PRECHARGE ALL command.

7. Wait at least ^{t}RP time; during this time, NOPs or DESELECT commands must be given. All banks will complete their precharge, thereby placing the device in the all banks idle state.
8. Issue an AUTO REFRESH command.
9. Wait at least ^{t}RFC time, during which only NOPs or COMMAND INHIBIT commands are allowed.
10. Issue an AUTO REFRESH command.
11. Wait at least ^{t}RFC time, during which only NOPs or COMMAND INHIBIT commands are allowed.
12. The SDRAM is now ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded with desired bit values prior to applying any operational command. Using the LMR command, program the mode register. The mode register is programmed via the MODE REGISTER SET command with BA1 = 0, BA0 = 0 and retains the stored information until it is programmed again or the device loses power. Not programming the mode register upon initialization will result in default settings which may not be desired. Outputs are guaranteed High-Z after the LMR command is issued. Outputs should be High-Z already before the LMR command is issued.
13. Wait at least ^{t}MRD time, during which only NOP or DESELECT commands are allowed.

At this point the DRAM is ready for any valid command.

Note: If desired, more than two AUTO REFRESH commands can be issued in the sequence. After steps 9 and 10 are complete, repeat them until the desired number of AUTO REFRESH + ^{t}RFC loops is achieved.

Register Definition

Mode Register

The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of BL, a burst type, CL, an operating mode, and a write burst mode, as shown in Figure 5 on page 14. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0–M2 specify BL, M3 specifies the type of burst (sequential or interleaved), M4–M6 specify CL, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 and M11 are reserved for future use. Address A12 (M12) is undefined but should be driven LOW during loading of the mode register.

The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length (BL)

Read and write accesses to the SDRAM are burst oriented, with BL being programmable, as shown in Figure 5 on page 14. BL determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used because unknown operation or incompatibility with future versions may result.

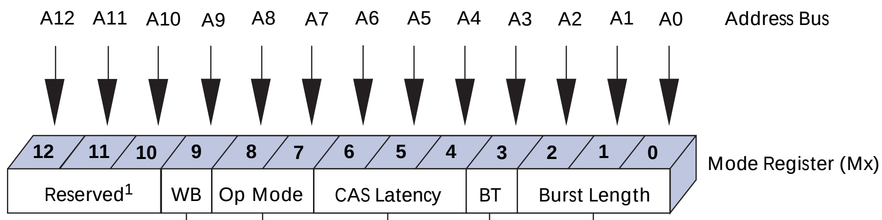
When a READ or WRITE command is issued, a block of columns equal to BL is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–A9, A11, A12 (x4); A1–A9, A11 (x8); or A1–A9 (x16) when BL = 2; by A2–A9, A11, A12 (x4); A2–A9, A11 (x8) or A2–A9 (x16) when the BL = 4; and by A3–A9, A11, A12 (x4); A3–A9, A11 (x8) or A3–A9 (x16) when the BL = 8. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

Burst Type

Accesses within a given burst may be programmed either to be sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by BL, the burst type and the starting column address, as shown in Table 4 on page 15.

Figure 5: Mode Register Definition



M9	Write Burst Mode
0	Programmed burst length
1	Single location access

M8	M7	M6-M0	Operating Mode
0	0	Defined	Standard operation
–	–	–	All other states reserved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

	Burst Length	
M2 M1 M0	M3 = 0	M3 = 1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

Notes: 1. Should program M12, M11, M10 = “0, 0, 0” to ensure compatibility with future devices.

Table 4: Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2	–	–	A0		
	–	–	0	0-1	0-1
	–	–	1	1-0	1-0
4	–	A1	A0		
	–	0	0	0-1-2-3	0-1-2-3
	–	0	1	1-2-3-0	1-0-3-2
	–	1	0	2-3-0-1	2-3-0-1
	–	1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full page (y)	n = A0–A12/11/9 (location 0–y)			Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4…, …Cn - 1, Cn…	Not supported

Notes:
1. For full-page accesses: y = 4,096 (x4); y = 2,048 (x8); y = 1,024 (x16).
2. For BL = 2, A1–A9, A11, A12 (x4); A1–A9, A11 (x8); or A1–A9 (x16) select the block-of-two burst; A0 selects the starting column within the block.
3. For BL = 4, A2–A9, A11, A12 (x4); A2–A9, A11 (x8); or A2–A9 (x16) select the block-of-four burst; A0–A1 select the starting column within the block.
4. For BL = 8, A3–A9, A11, A12 (x4); A3–A9, A11 (x8); or A3–A9 (x16) select the block-of-eight burst; A0–A2 select the starting column within the block.
5. For a full-page burst, the full row is selected and A0–A9, A11, A12 (x4); A0–A9, A11 (x8); or A0–A9 (x16) select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For BL = 1, A0–A9, A11, A12 (x4); A0–A9, A11 (x8); or A0–A9 (x16) select the unique column to be accessed, and mode register bit M3 is ignored.

CAS Latency (CL)

CL is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge n and the latency is m clocks, the data will be available by clock edge $n + m$. The DQs will start driving as a result of the clock edge one cycle earlier ($n + m - 1$), and provided that the relevant access times are met, the data will be valid by clock edge $n + m$. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the

latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 6. Table 5 indicates the operating frequencies at which each CL setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Figure 6: CAS Latency

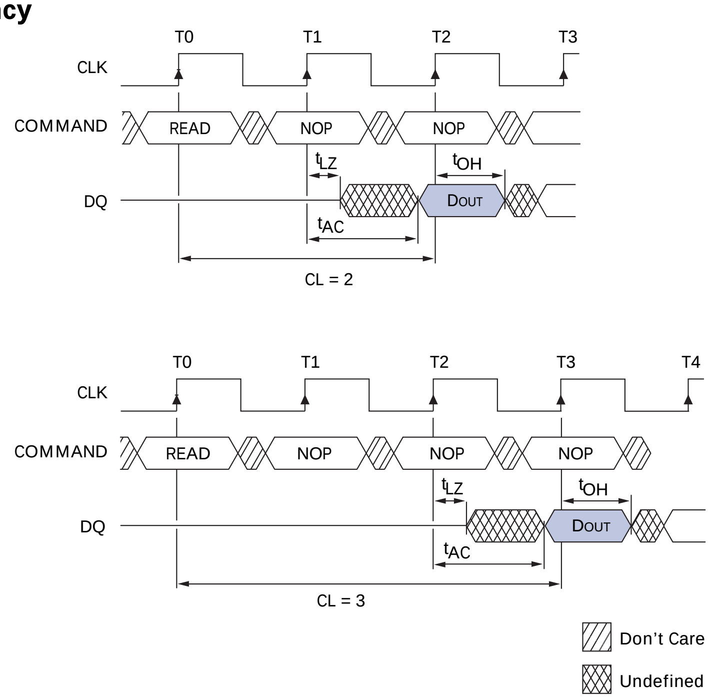


Table 5: CAS Latency

Speed	Allowable Operating Frequency (MHz)	
	CL = 2	CL = 3
-7E	≤ 133	≤ 143
-75	≤ 100	≤ 133

Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

WRITE Burst Mode

When M9 = 0, BL programmed via M0–M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

Commands

Table 6 provides a quick reference of available commands. This is followed by a written description of each command. Three additional Truth Tables appear in the Operations section, beginning on page 35; these tables provide current state/next state information.

Table 6: Truth Table 1 – Commands and DQM Operation
Notes 1–2 apply to entire table; notes appear below

Name (Function)	CS#	RAS#	CAS#	WE#	DQM	Address	DQs	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H[8]	Bank/col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H[8]	Bank/col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X	4
Write enable/output enable	–	–	–	–	L	–	Active	8
Write inhibit/output High-Z	–	–	–	–	H	–	High-Z	8

Notes:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A0–A11 define the op-code written to the mode register, and A12 should be driven LOW.
3. A0–A12 provide row address, and BA0, BA1 determine which bank is made active.
4. A0–A9, A11, A12 (x4); A0–A9, A11 (x8); or A0–A9 (x16) provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which bank is being read from or written to.
5. A10 LOW: BA0, BA1 determine the bank being precharged. A10 HIGH: All banks precharged and BA0, BA1 are “Don’t Care.”
6. This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
8. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay).

COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an SDRAM that is selected (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode register is loaded via inputs A0–A11 (A12 should be driven LOW). See "Mode Register" on page 13. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A12 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A9, A11, A12 (x4); A0–A9, A11 (x8); or A0–A9 (x16) selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Read data appears on the DQs subject to the logic level on the DQM inputs two clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQs will be High-Z two clocks later; if the DQM signal was registered LOW, the DQs will provide valid data.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A9, A11, A12 (x4); A0–A9, A11 (x8); or A0–A9 (x16) selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Auto Precharge

Auto precharge is a feature that performs the same individual-bank PRECHARGE function described above, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A PRECHARGE of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst, except in the full-page burst mode, where auto precharge does not apply. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (^tRP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the "Operations" section on page 20.

BURST TERMINATE

The BURST TERMINATE command is used to truncate either fixed-length or full-page bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated, as shown in the "Operations" section on page 20. The BURST TERMINATE command does not precharge the row; the row will remain open until a PRECHARGE command is issued.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) REFRESH in conventional DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. All active banks must be PRECHARGED prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum ^tRP has been met after the PRECHARGE command as shown in the "Operations" section on page 20.

The addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command. The 512Mb SDRAM requires 8,192 AUTO REFRESH cycles every 64ms (^tREF), regardless of width option. Providing a distributed AUTO REFRESH command every 7.81µs will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 8,192 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (^tRC), once every 64ms.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). After the SELF REFRESH command is registered, all the inputs to the SDRAM become "Don't Care" with the exception of CKE, which must remain LOW.

After self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own AUTO REFRESH cycles. The SDRAM must remain in self refresh mode for a minimum period equal to ^tRAS and may remain in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) prior to CKE going back HIGH. When CKE is HIGH, the SDRAM must have NOP commands issued (a minimum of two clocks) for ^{t}XSR because time is required for the completion of any internal refresh in progress.

Upon exiting the self refresh mode, AUTO REFRESH commands must be issued every 7.81µs or less as both SELF REFRESH and AUTO REFRESH utilize the row refresh counter.

Operations

Bank/Row Activation

Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated (see Figure 7).

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a ^{t}RCD specification of 20ns with a 125 MHz clock (8ns period) results in 2.5 clocks, rounded to 3. This is reflected in Figure 8 on page 21, which covers any case where $2 < {}^{t}RCD (MIN)/{}^{t}CK \leq 3$ (the same procedure is used to convert other specification limits from time units to clock cycles). A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

Figure 7: Activating a Specific Row In a Specific Bank

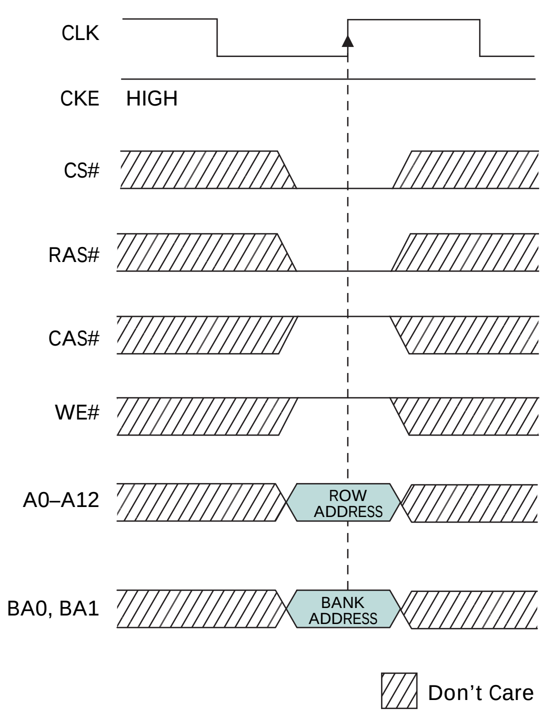
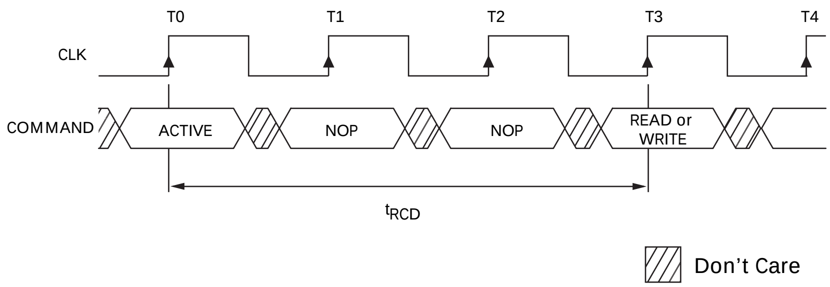


Figure 8: Example Meeting ^{t}RCD (MIN) when 2 < ^{t}RCD (MIN)/^{t}CK ≤ 3



READs

READ bursts are initiated with a READ command, as shown in Figure 9.

The starting column and bank addresses are provided with the READ command, and auto precharge either is enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following CL after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 10 on page 22 shows general timing for each possible CL setting.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

Figure 9: READ Command

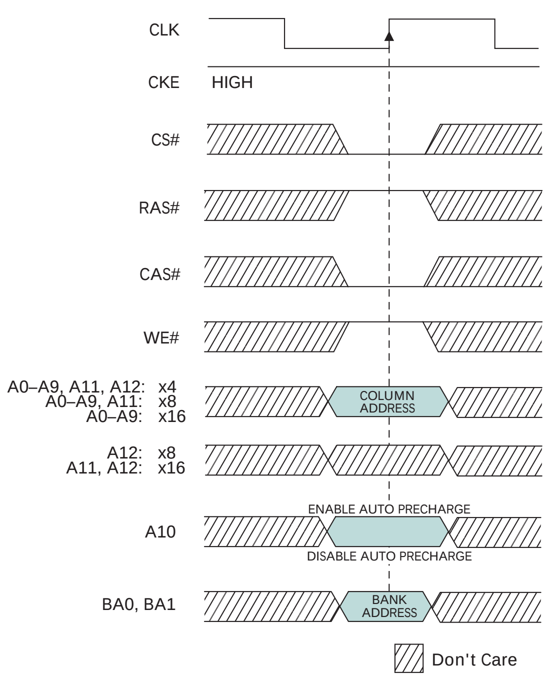
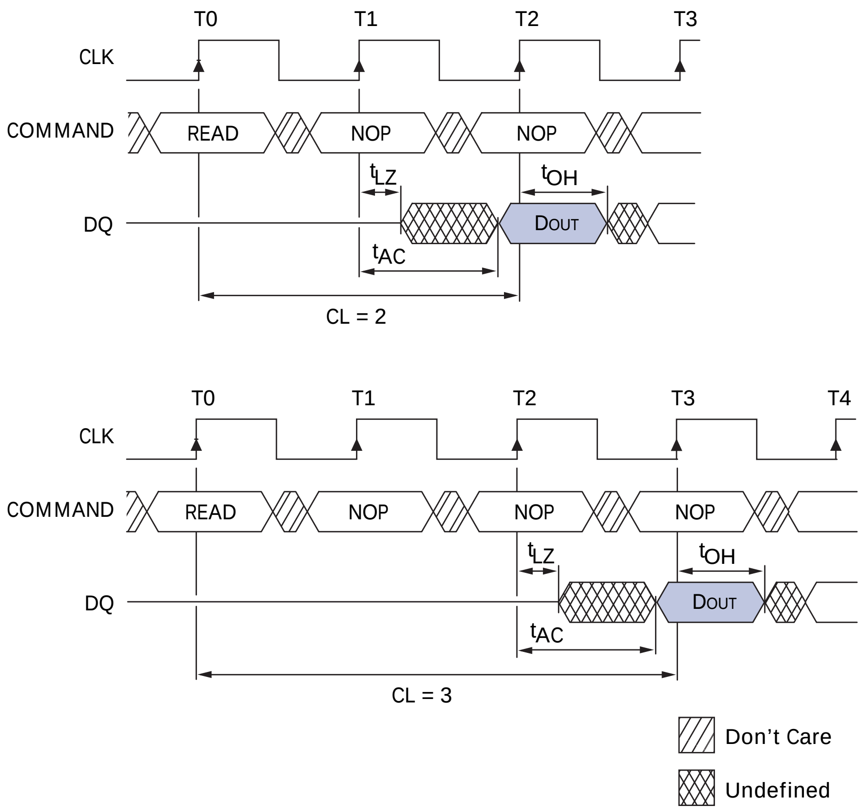


Figure 10: CAS Latency

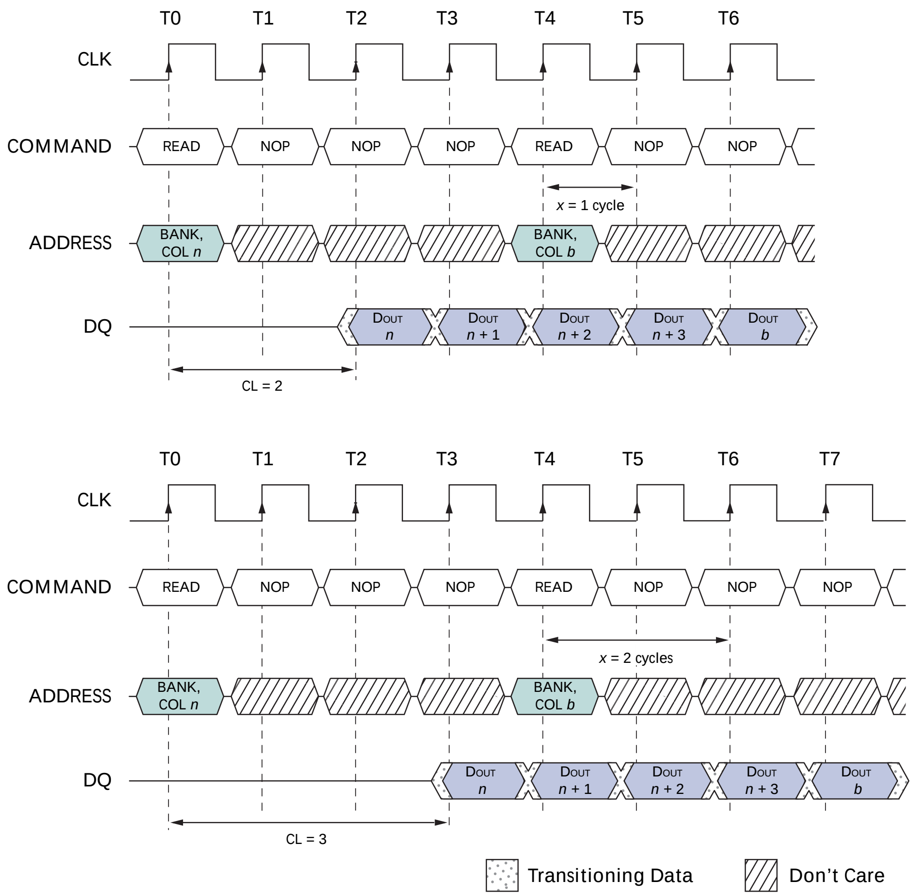


Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A full-page burst will continue until terminated (at the end of the page, it will wrap to the start address and continue). Data from any READ burst may be truncated with a subsequent READ command, and data from a fixed-length READ burst may be immediately followed by data from a READ command.

In either case, a continuous flow of data can be maintained. The first data element from the new burst either follows the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new READ command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where x = CL - 1. This is shown in Figure 10 for CL = 2 and CL = 3; data element $n + 3$ is either the last of a burst of four or the last desired of a longer burst.

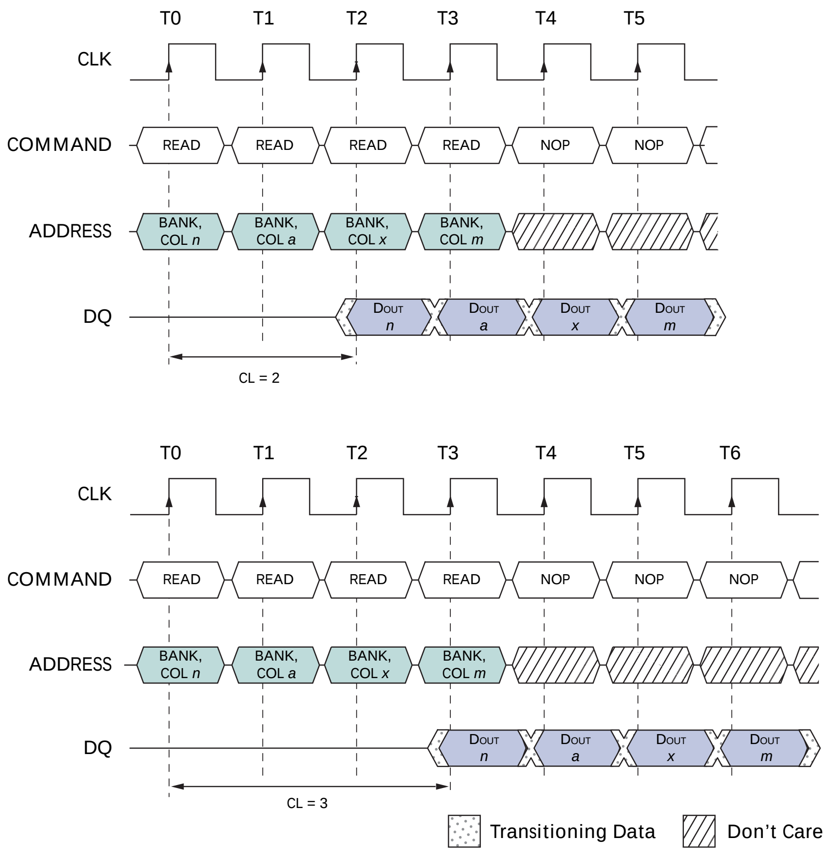
The 512Mb SDRAM uses a pipelined architecture and therefore does not require the 2*n* rule associated with a prefetch architecture. A READ command can be initiated on any clock cycle following a previous READ command. Full-speed random read accesses can be performed to the same bank, as shown in Figure 12 on page 24, or each subsequent READ may be performed to a different bank.

Figure 11: Consecutive READ Bursts



Note: Each READ command may be to any bank. DQM is LOW.

Figure 12: Random READ Accesses



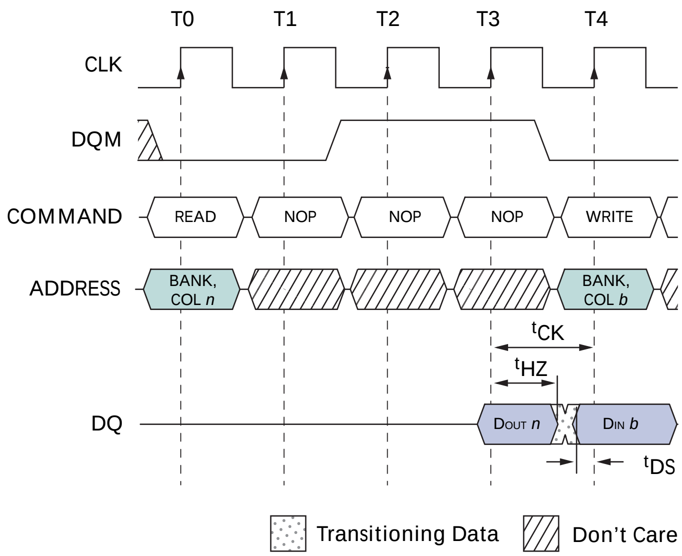
Note: Each READ command may be to any bank. DQM is LOW.

Data from any READ burst may be truncated with a subsequent WRITE command, and data from a fixed-length READ burst may be immediately followed by data from a WRITE command (subject to bus turnaround limitations). The WRITE burst may be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. In a given system design, there may be a possibility that the device driving the input data will go Low-Z before the SDRAM DQs go High-Z. In this case, at least a single-cycle delay should occur between the last read data and the WRITE command.

The DQM input is used to avoid I/O contention, as shown in Figure 13 on page 25 and Figure 14 on page 25. The DQM signal must be asserted (HIGH) at least two clocks prior to the WRITE command (DQM latency is two clocks for output buffers) to suppress data-out from the READ. After the WRITE command is registered, the DQs will go High-Z (or remain High-Z), regardless of the state of the DQM signal, provided the DQM was active on the clock just prior to the WRITE command that truncated the READ command. If not, the second WRITE will be an invalid WRITE. For example, if DQM was LOW during T4 in Figure 14 on page 25, then the WRITEs at T5 and T7 would be valid, while the WRITE at T6 would be invalid.

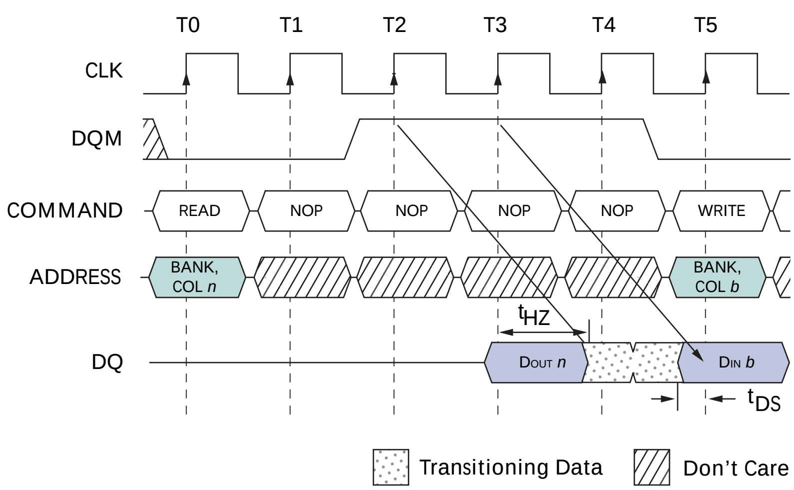
The DQM signal must be de-asserted prior to the WRITE command (DQM latency is zero clocks for input buffers) to ensure that the written data is not masked. Figure 13 shows the case where the clock frequency allows for bus contention to be avoided without adding a NOP cycle, and Figure 14 shows the case where the additional NOP is needed.

Figure 13: READ-to-WRITE



Note: A CL = 3 is used for illustration. The READ command may be to any bank, and the WRITE command may be to any bank. If a burst of 1 is used, then DQM is not required.

Figure 14: READ-to-WRITE with Extra Clock Cycle



Note: CL = 3 is used for illustration. The READ command may be to any bank, and the WRITE command may be to any bank.

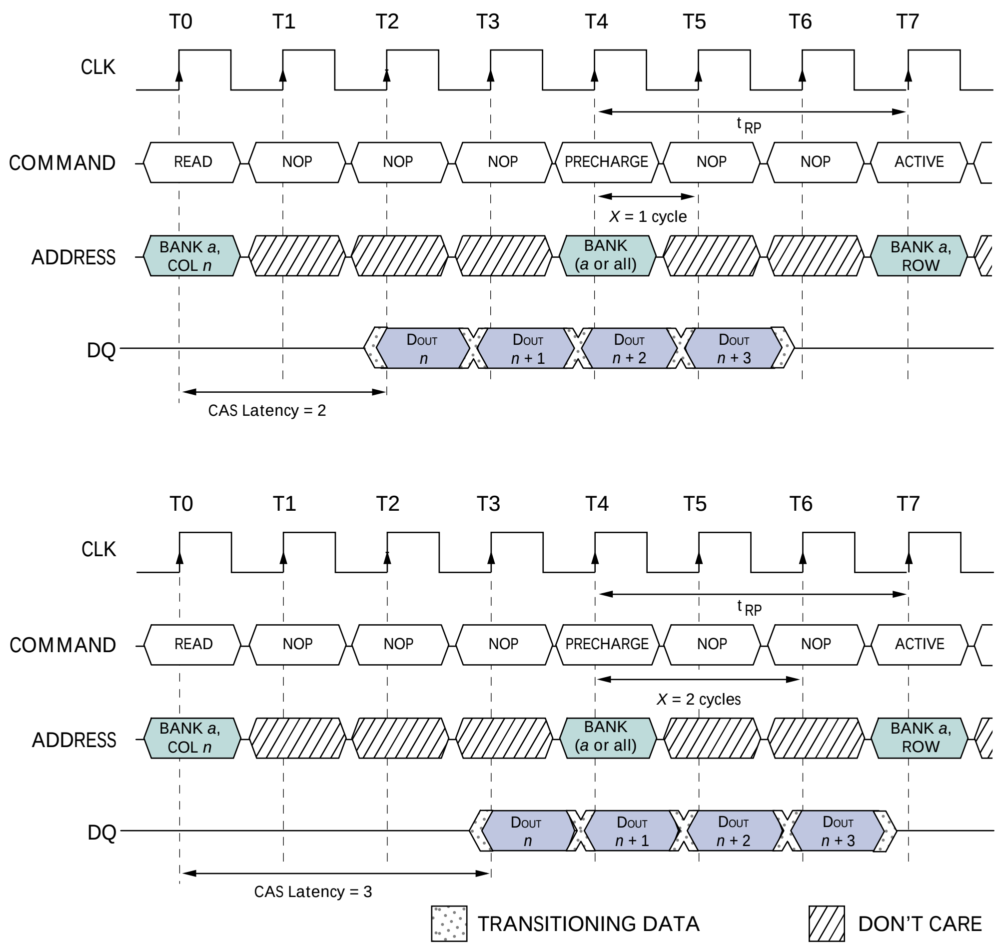
A fixed-length READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated), and a full-page burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where x = CL - 1. This is shown in Figure 15 on page 26 for

each possible CL; data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met. Note that part of the row precharge time is hidden during the access of the last data element(s).

In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or full-page bursts.

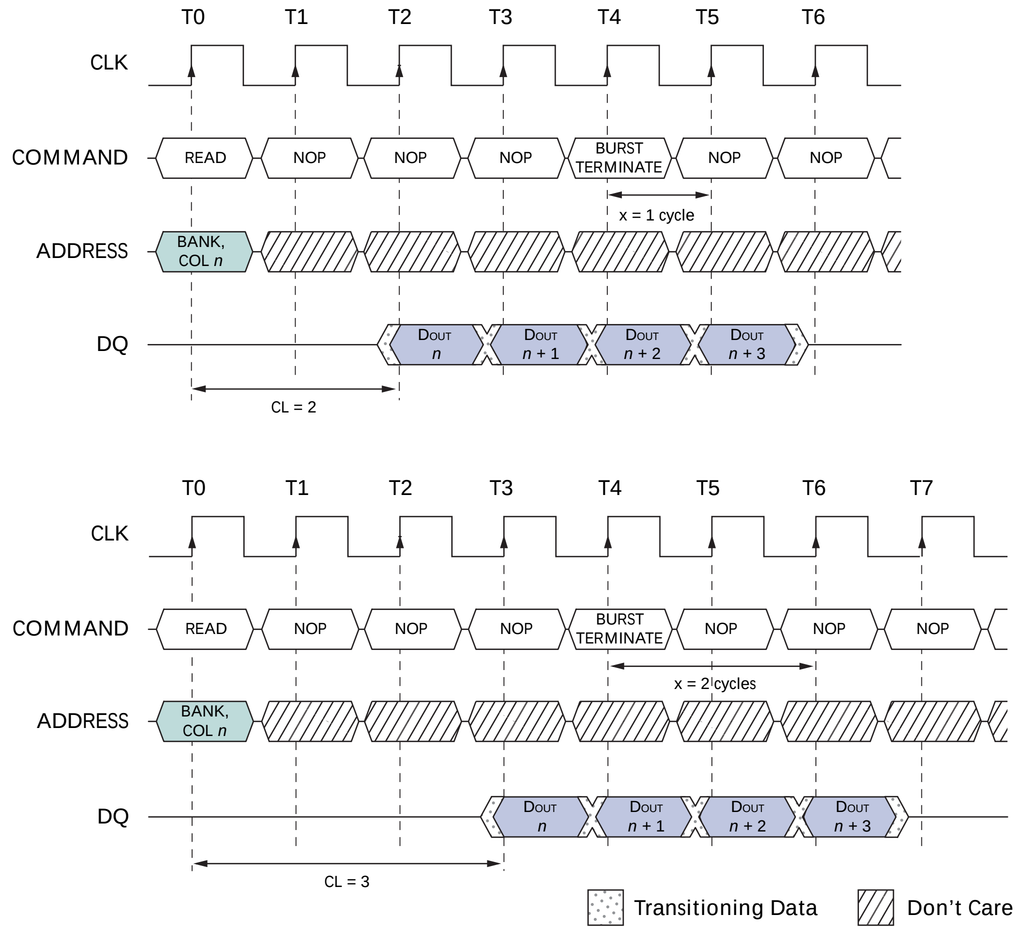
Full-page READ bursts can be truncated with the BURST TERMINATE command, and fixed-length READ bursts may be truncated with a BURST TERMINATE command, provided that auto precharge was not activated. The BURST TERMINATE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* = CL - 1. This is shown in Figure 16 on page 27 for each possible CL; data element *n* + 3 is the last desired data element of a longer burst.

Figure 15: READ-to-PRECHARGE



NOTE: DQM is LOW.

Figure 16: Terminating a READ Burst



Note: DQM is LOW.

WRITEs

WRITE bursts are initiated with a WRITE command, as shown in Figure 17.

The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered coincident with the WRITE command. Subsequent data elements will be registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored (see Figure 18 on page 29). A full-page burst will continue until terminated (at the end of the page, it will wrap to the start address and continue). Data for any WRITE burst may be truncated with a subsequent WRITE command, and data for a fixed-length WRITE burst may be immediately followed by data for a WRITE command. The new WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command. An example is shown in Figure 19 on page 29. Data n + 1 is either the last of a burst of two or the last desired of a longer burst. The 512Mb SDRAM uses a pipelined architecture and therefore does not require the 2n rule associated with a prefetch architecture. A WRITE command can be initiated on any clock cycle following a previous WRITE command. Full-speed random write accesses within a page can be performed to the same bank, as shown in Figure 20 on page 30, or each subsequent WRITE may be performed to a different bank.

Figure 17: WRITE Command

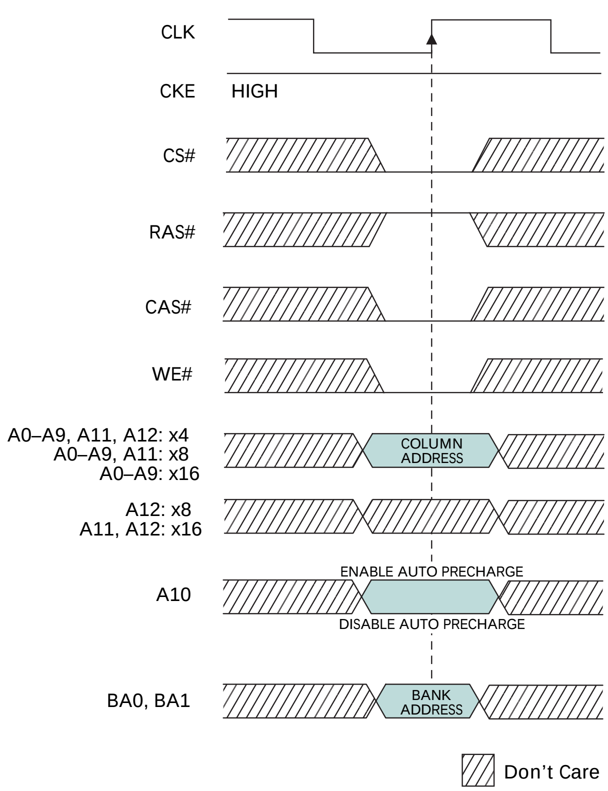
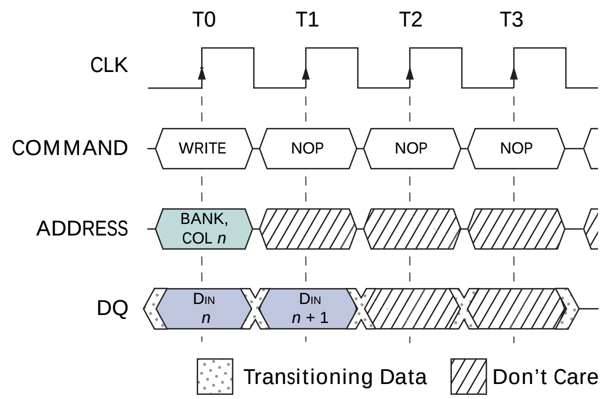


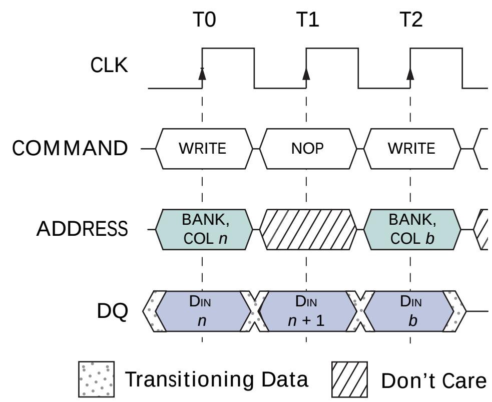
Figure 18: WRITE Burst



Note: BL = 2. DQM is LOW.

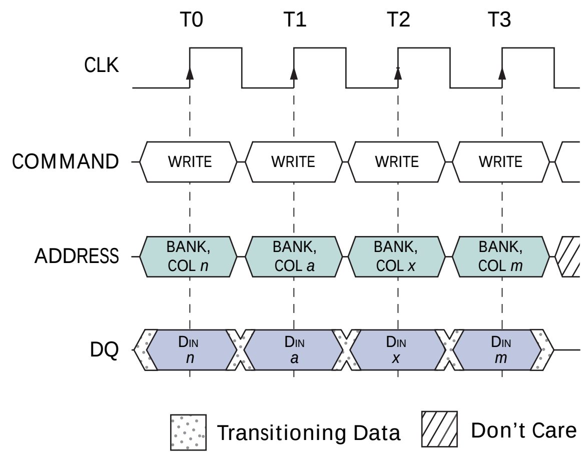
Data for any WRITE burst may be truncated with a subsequent READ command, and data for a fixed-length WRITE burst may be immediately followed by a READ command. After the READ command is registered, the data inputs will be ignored, and WRITEs will not be executed. An example is shown in Figure 21 on page 30. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst.

Figure 19: WRITE-to-WRITE



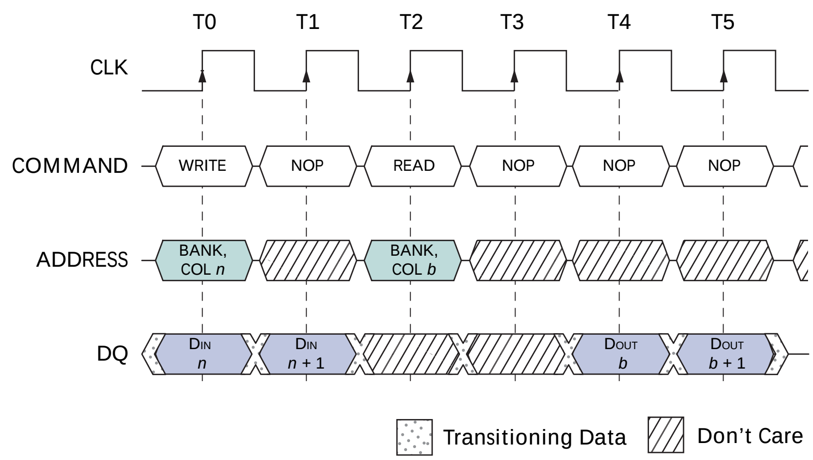
Note: DQM is LOW. Each WRITE command may be to any bank.

Figure 20: Random WRITE Cycles



Note: Each WRITE command may be to any bank. DQM is LOW.

Figure 21: WRITE-to-READ



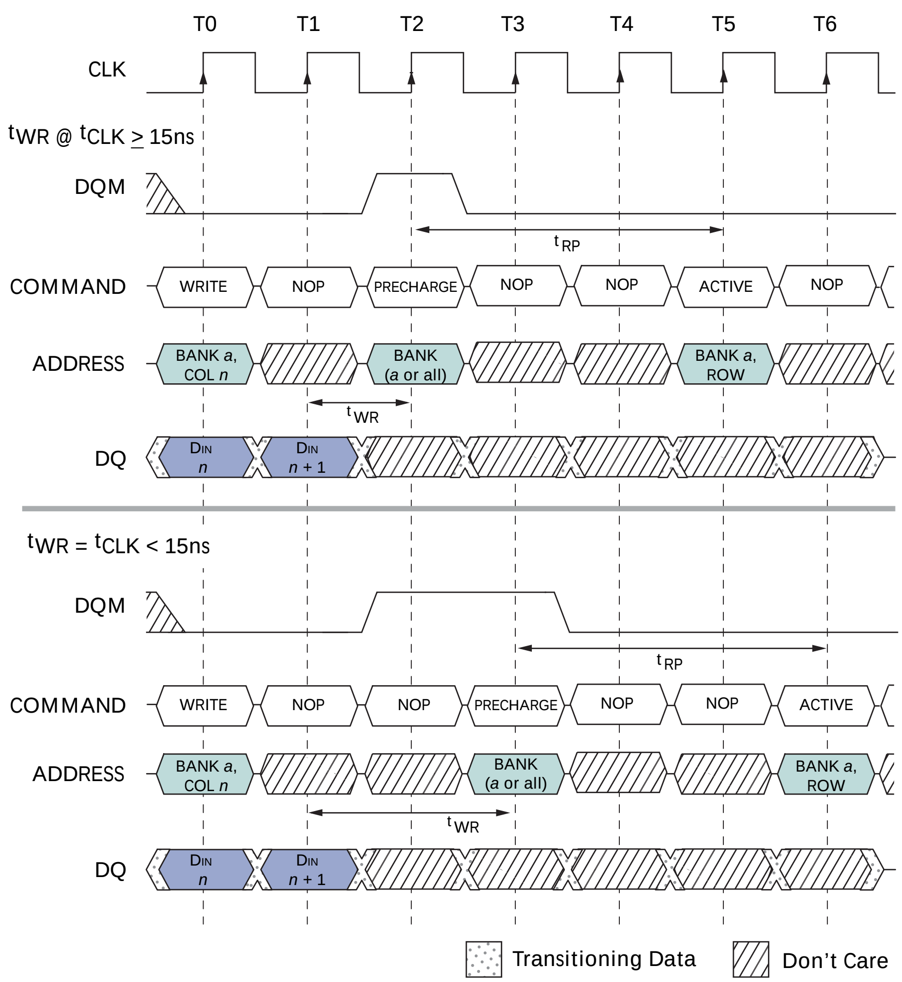
Note: The WRITE or READ commands may be to any bank. DQM is LOW.

Data for a fixed-length WRITE burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated), and a full-page WRITE burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued ^{t}WR after the clock edge at which the last desired input data element is registered. The auto precharge mode requires a ^{t}WR of at least one clock plus time, regardless of frequency. In addition, when truncating a WRITE burst, the DQM signal must be used to mask input data for the clock edge prior to, and the clock edge coincident with, the PRECHARGE command. An example is shown in Figure 22 on page 31. Data $n + 1$ is either the last of a burst of two or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met. The precharge can be issued coincident with the first coincident second clock (Figure 22 on page 31). In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of

the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or full-page bursts.

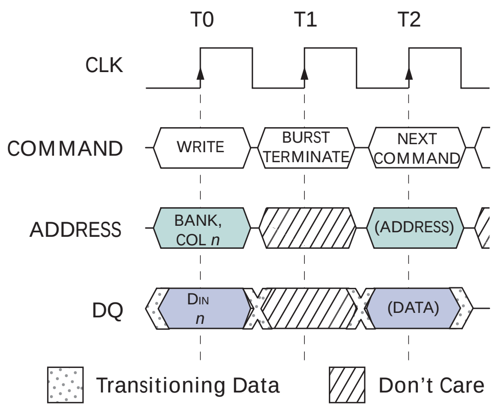
Fixed-length or full-page WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied coincident with the BURST TERMINATE command will be ignored. The last data written (provided that DQM is LOW at that time) will be the input data applied one clock previous to the BURST TERMINATE command. This is shown in Figure 23 on page 32, where data *n* is the last desired data element of a longer burst.

Figure 22: WRITE-to-PRECHARGE



Note: DQM could remain LOW in this example if the WRITE burst is a fixed length of two.

Figure 23: Terminating a WRITE Burst

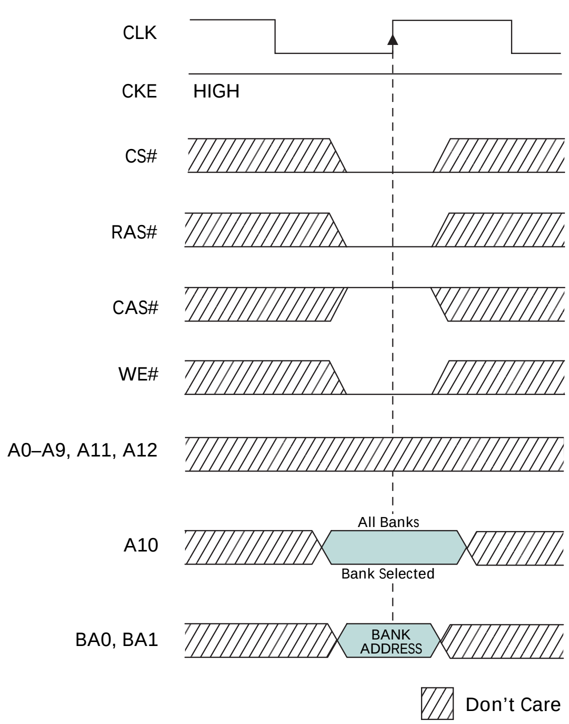


Note: DQMs are LOW.

PRECHARGE

The PRECHARGE command shown in Figure 24 is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (^tRP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Figure 24: PRECHARGE Command

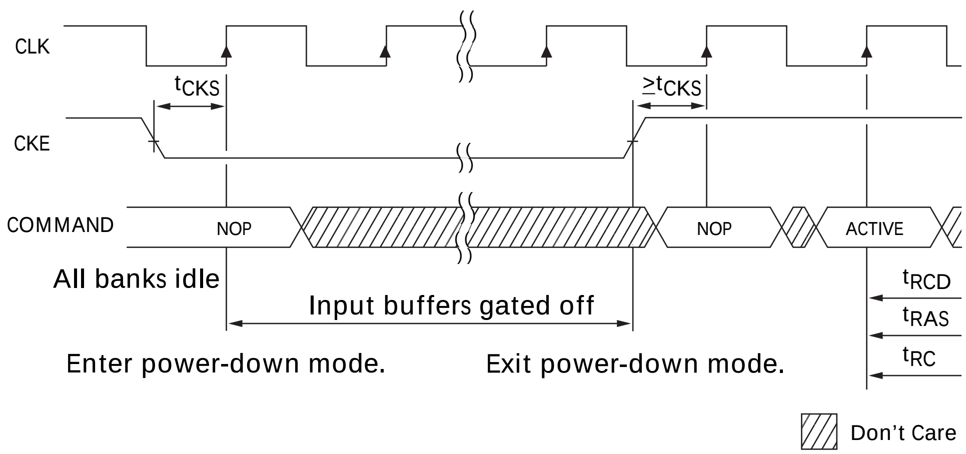


Power-Down

Power-down occurs if CKE is registered LOW coincident with a NOP or COMMAND INHIBIT when no accesses are in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device may not remain in the power-down state longer than the refresh period (64ms) since no refresh operations are performed in this mode.

The power-down state is exited by registering a NOP or COMMAND INHIBIT and CKE HIGH at the desired clock edge (meeting ^{t}CKS). See Figure 25.

Figure 25: Power-Down



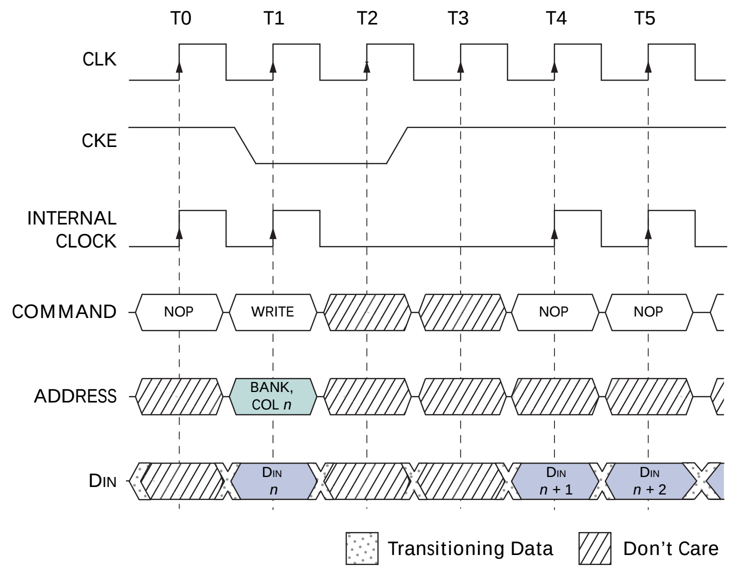
Clock Suspend

The clock suspend mode occurs when a column access/burst is in progress and CKE is registered LOW. In the clock suspend mode, the internal clock is deactivated, "freezing" the synchronous logic.

For each positive clock edge on which CKE is sampled LOW, the next internal positive clock edge is suspended. Any command or data present on the input pins at the time of a suspended internal clock edge is ignored; any data present on the DQ pins remains driven; and burst counters are not incremented, as long as the clock is suspended (see examples in Figures 26 and 27 on page 34).

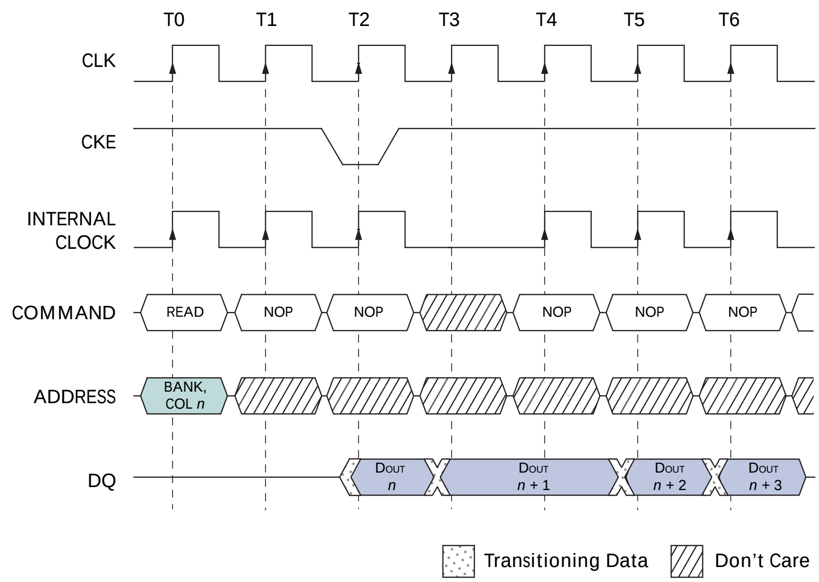
Clock suspend mode is exited by registering CKE HIGH; the internal clock and related operation will resume on the subsequent positive clock edge.

Figure 26: CLOCK SUSPEND During WRITE Burst



Note: BL = 4 or greater. DM is LOW.

Figure 27: CLOCK SUSPEND During READ Burst



Note: CL = 2, BL = 4 or greater. DQM is LOW.

Burst READ/Single WRITE

The burst read/single write mode is entered by programming the write burst mode bit (M9) in the mode register to a logic 1. In this mode, all WRITE commands result in the access of a single column location (burst of one), regardless of the programmed burst length. READ commands access columns according to the programmed burst length and sequence, just as in the normal mode of operation (M9 = 0).

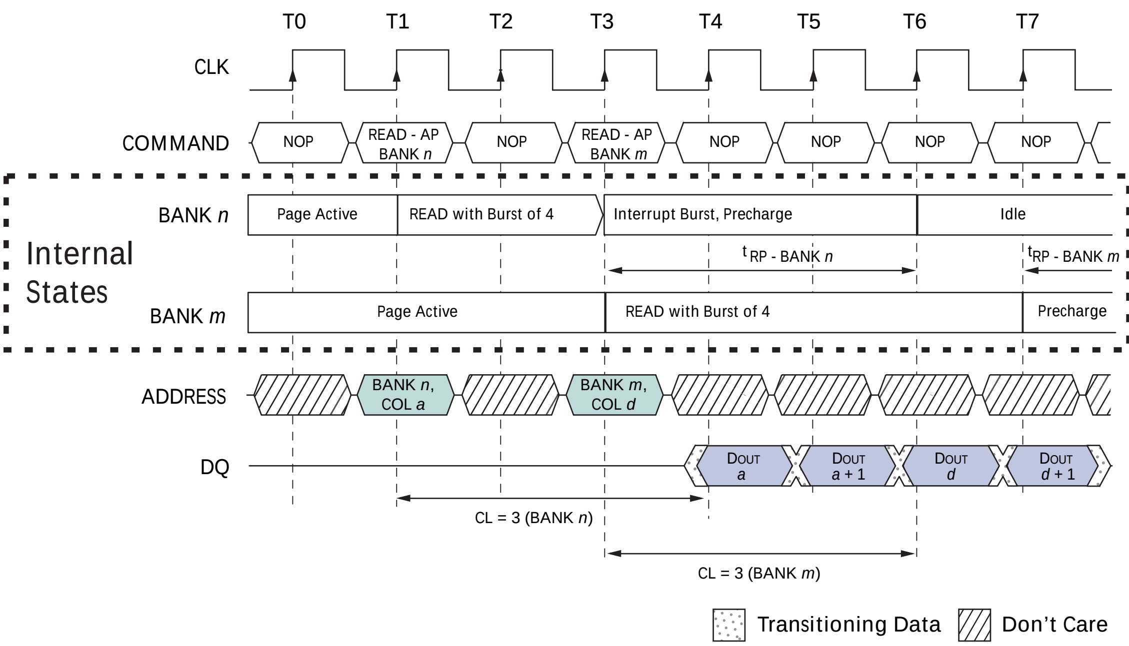
Concurrent Auto Precharge

An access command to (READ or WRITE) another bank while an access command with auto precharge enabled is executing is not allowed by SDRAMs, unless the SDRAM supports concurrent auto precharge. Micron SDRAMs support concurrent auto precharge. Four cases where concurrent auto precharge occurs are defined below.

READ with Auto Precharge

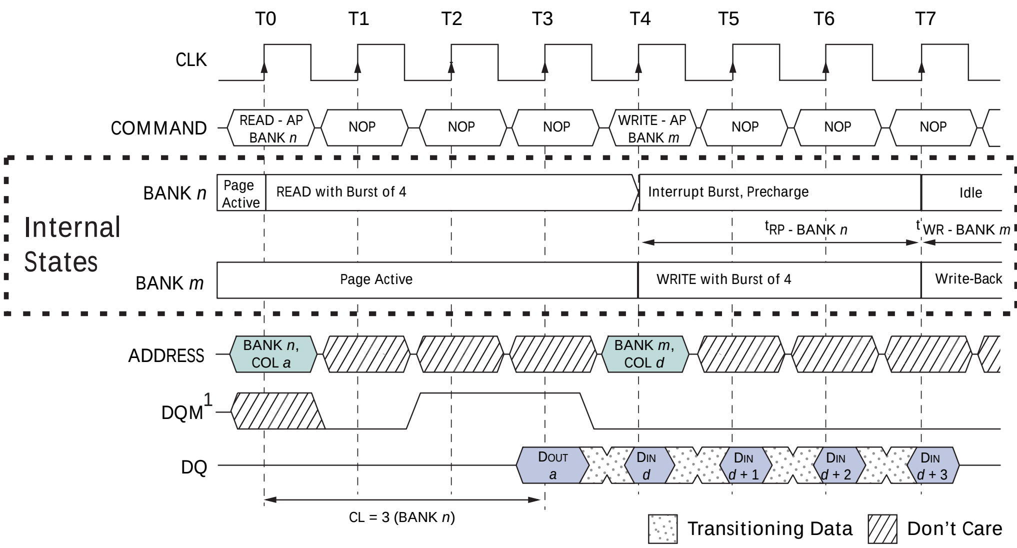
- Interrupted by a READ (with or without auto precharge): A READ to bank *m* will interrupt a READ on bank *n*, CL later. The PRECHARGE to bank *n* will begin when the READ to bank *m* is registered (see Figure 28).
- Interrupted by a WRITE (with or without auto precharge): A WRITE to bank *m* will interrupt a READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank *n* will begin when the WRITE to bank *m* is registered (see Figure 29 on page 36).

Figure 28: READ with Auto Precharge Interrupted by a READ



Note: DQM is LOW.

Figure 29: READ with Auto Precharge Interrupted by a WRITE

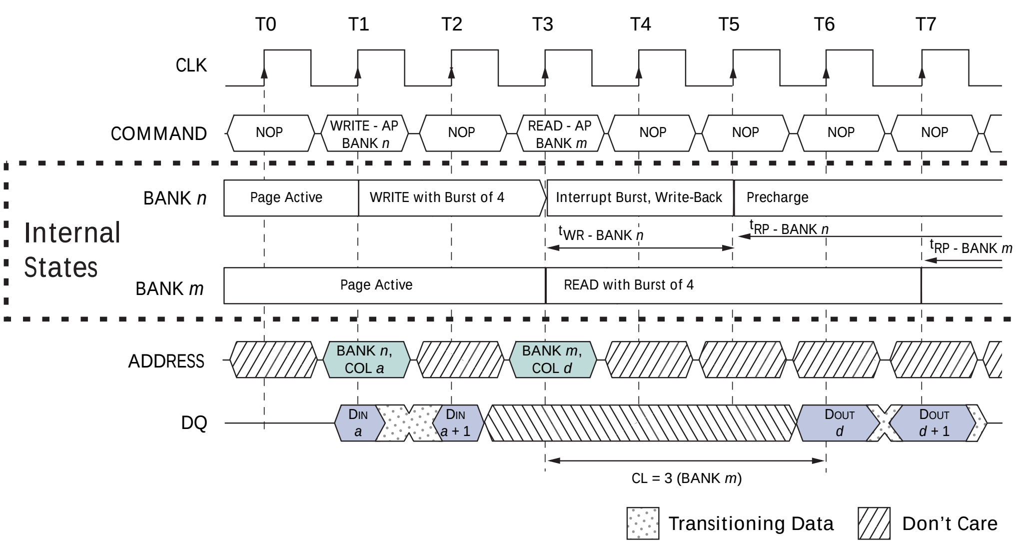


Notes: 1. DQM is HIGH at T2 to prevent DOUT - *a* + 1 from contending with DIN - *d* at T4.

WRITE with Auto Precharge

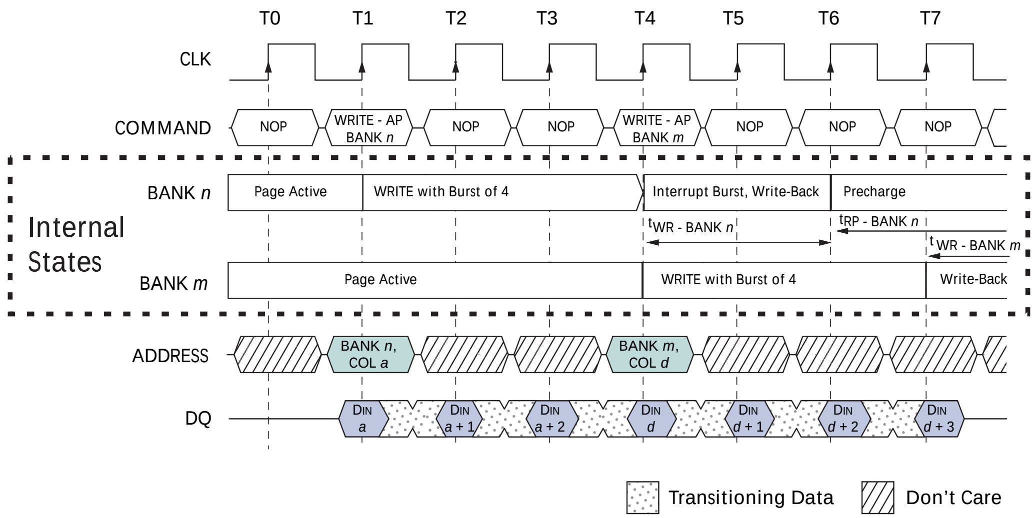
- Interrupted by a READ (with or without auto precharge): A READ to bank *m* will interrupt a WRITE on bank *n* when registered, with the data-out appearing CL later. The PRECHARGE to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the READ to bank *m* is registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m* (see Figure 30).
- Interrupted by a WRITE (with or without auto precharge): A WRITE to bank *m* will interrupt a WRITE on bank *n* when registered. The PRECHARGE to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the WRITE to bank *m* is registered. The last valid data WRITE to bank *n* will be data registered one clock prior to a WRITE to bank *m* (see Figure 31 on page 37).

Figure 30: WRITE with Auto Precharge Interrupted by a READ



Note: DQM is LOW.

Figure 31: WRITE with Auto Precharge Interrupted by a WRITE



Note: DQM is LOW.

Table 7: Truth Table 2 – CKE
Notes 1–4 apply to entire table; notes appear below

CKE_{n-1}	CKE_n	Current State	$COMMAND_n$	$ACTION_n$	Notes
L	L	Power-down	X	Maintain power-down	
		Self refresh	X	Maintain self refresh	
		Clock suspend	X	Maintain clock suspend	
L	H	Power-down	COMMAND INHIBIT or NOP	Exit power-down	5
		Self refresh	COMMAND INHIBIT or NOP	Exit self refresh	6
		Clock suspend	X	Exit clock suspend	7
H	L	All banks idle	COMMAND INHIBIT or NOP	Power-down entry	
		All Banks idle	AUTO REFRESH	Self refresh entry	
		Reading or writing	WRITE or NOP	Clock suspend entry	
H	H		See Table 8 on page 38		

Notes:
1. CKE_n is the logic state of CKE at clock edge *n*; CKE_{n-1} was the state of CKE at the previous clock edge.
2. Current state is the state of the SDRAM immediately prior to clock edge *n*.
3. $COMMAND_n$ is the command registered at clock edge *n*, and $ACTION_n$ is a result of $COMMAND_n$.
4. All states and sequences not shown are illegal or reserved.
5. Exiting power-down at clock edge *n* will put the device in the all banks idle state in time for clock edge *n* + 1 (provided that ^{t}CKS is met).
6. Exiting self refresh at clock edge n will put the device in the all banks idle state once ^{t}XSR is met. COMMAND INHIBIT or NOP commands should be issued on any clock edges occurring during the ^{t}XSR period. A minimum of two NOP commands must be provided during ^{t}XSR period.
7. After exiting clock suspend at clock edge n, the device will resume operation and recognize the next command at clock edge *n* + 1.

Table 8: Truth Table 3 – Current State Bank *n*, Command to Bank *n*
Notes: 1–6 apply to entire table; notes appear below and on next page

Current State	CS#	RAS#	CAS#	WE#	Command (Action)	Notes
Any	H	X	X	X	COMMAND INHIBIT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (Select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
	L	L	H	L	PRECHARGE	11
Row active	L	H	L	H	READ (Select column and start READ burst)	10
	L	H	L	L	WRITE (Select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	8
Read (auto precharge disabled)	L	H	L	H	READ (Select column and start new READ burst)	10
	L	H	L	L	WRITE (Select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (Truncate READ burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9
Write (auto precharge disabled)	L	H	L	H	READ (Select column and start READ burst)	10
	L	H	L	L	WRITE (Select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (Truncate WRITE burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9

Notes:
1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see Table 7 on page 37) and after ^tXSR has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted, that is, the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and ^tRP has been met.

   Row active: A row in the bank has been activated, and ^tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table 8 and according to Table 9 on page 40.

   Precharging: Starts with registration of a PRECHARGE command and ends when ^tRP is met. After ^tRP is met, the bank will be in the idle state.

   Row activating: Starts with registration of an ACTIVE command and ends when ^tRCD is met. After ^tRCD is met, the bank will be in the row active state.

   Read with auto precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when ^tRP has been met. After ^tRP is met, the bank will be in the idle state.

   Write w/auto precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when ^tRP has been met. After ^tRP is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.

Refreshing:	Starts with registration of an AUTO REFRESH command and ends when ^tRC is met. After ^tRC is met, the SDRAM will be in the all banks idle state.
Accessing mode register:	Starts with registration of a LOAD MODE REGISTER command and ends when ^tMRD has been met. After ^tMRD is met, the SDRAM will be in the all banks idle state.
Precharging all:	Starts with registration of a PRECHARGE ALL command and ends when ^tRP is met. After ^tRP is met, all banks will be in the idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle.
8. May or may not be bank-specific; if all banks are to be precharged, all must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ or WRITE burst, regardless of bank.
10. READs or WRITEs listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Does not affect the state of the bank and acts as a NOP to that bank.

Table 9: Truth Table 4 – Current State Bank *n*, Command to Bank *m*

Notes 1–6 apply to entire table; notes appear below and on next page

Current State	CS#	RAS#	CAS#	WE#	Command (Action)	Notes
Any	H	X	X	X	COMMAND INHIBIT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any command otherwise allowed to bank *m*	
Row activating, active, or precharging	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7
	L	H	L	L	WRITE (Select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge disabled)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	7, 10
	L	H	L	L	WRITE (Select column and start WRITE burst)	7, 11
	L	L	H	L	PRECHARGE	9
Write (auto precharge disabled)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7, 12
	L	H	L	L	WRITE (Select column and start new WRITE burst)	7, 13
	L	L	H	L	PRECHARGE	9
Read (with auto precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	7, 8, 14
	L	H	L	L	WRITE (Select column and start WRITE burst)	7, 8, 15
	L	L	H	L	PRECHARGE	9
Write (with auto precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7, 8, 16
	L	H	L	L	WRITE (Select column and start new WRITE burst)	7, 8, 17
	L	L	H	L	PRECHARGE	9

Notes:

1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see Table 7 on page 37) and after ^tXSR has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted; that is, the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m* (assuming that bank *m* is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and ^tRP has been met.

   Row active: A row in the bank has been activated, and ^tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Read with auto precharge enabled: Starts with registration of a READ command with auto precharge enabled, and ends when ^tRP has been met. After ^tRP is met, the bank will be in the idle state.

   Write with auto precharge enabled: Starts with registration of a WRITE command with auto precharge enabled, and ends when ^tRP has been met. After ^tRP is met, the bank will be in the idle state.

4. AUTO REFRESH, SELF REFRESH, and LOAD MODE REGISTER commands may only be issued when all banks are idle.

5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs to bank *m* listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. Concurrent auto precharge: Bank *n* will initiate the auto precharge command when its burst has been interrupted by bank *m*'s burst.
9. Burst in bank *n* continues as initiated.
10. For a READ without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CL later (Figure 11 on page 23).
11. For a READ without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered (Figure 13 and Figure 14 on page 25). DQM should be used one clock prior to the WRITE command to prevent bus contention.
12. For a WRITE without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered (Figure 21 on page 30), with the data-out appearing CL later. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
13. For a WRITE without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the WRITE on bank *n* when registered (Figure 19 on page 29). The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
14. For a READ with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CL later. The PRECHARGE to bank *n* will begin when the READ to bank *m* is registered (Figure 28 on page 35).
15. For a READ with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank *n* will begin when the WRITE to bank *m* is registered (Figure 29 on page 36).
16. For a WRITE with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered, with the data-out appearing CL later. The PRECHARGE to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the READ to bank *m* is registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m* (Figure 30 on page 36).
17. For a WRITE with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the WRITE on bank *n* when registered. The PRECHARGE to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the WRITE to bank *m* is registered. The last valid WRITE to bank *n* will be data registered one clock prior to the WRITE to bank *m* (Figure 31 on page 37).

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 10: Absolute Maximum Ratings

Parameter	Symbol		Min	Max	Units	Notes
VDD supply voltage relative to VSS	VDD		–1.0	+4.6	V	
VDDQ supply voltage relative to VSS	VDDQ		–1.0	+4.6	V	
Voltage on any pin relative to VSS	VIN, VOUT, NC		–1.0	+4.6	V	
SDRAM device temperatures	T_A	Commercial	0	+70	°C	1
		Industrial	–40	+85	°C	1
		Storage (plastic)	–55	+155	°C	1
Power dissipation	–		–	+1	W	

Note: For further information, refer to technical note TN-00-08: Thermal Applications, available on Micron's Web site.

Temperature and Thermal Impedance

It is imperative that the SDRAM device's temperature specifications, shown in Table 11 on page 43, be maintained to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. The thermal impedances are listed in Table 12 on page 43 for the applicable die revision and packages being made available. These thermal impedance values vary according to the density, package, and particular design used for each device.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08, "Thermal Applications" prior to using the thermal impedances listed in Table 12 on page 43. To ensure the compatibility of current and future designs, contact Micron Applications Engineering to confirm thermal impedance values. The SDRAM device's safe junction temperature range can be maintained when the T_C specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required to satisfy the case temperature specifications.

Table 11: Temperature Limits

Parameter	Symbol	Min	Max	Units	Notes
Operating case temperature: Commercial Industrial	T_C	 0 –40	 80 90	°C	1, 2, 3, 4
Junction temperature: Commercial Industrial	T_J	 0 –40	 85 95	°C	3
Ambient temperature: Commercial Industrial	T_A	 0 –40	 70 85	°C	3, 5
Peak reflow temperature	T_{PEAK}	–	260	°C	

Notes:
1. MAX operating case temperature, T_C, is measured in the center of the package on the top side of the device, as shown on page 47.
2. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
3. Both temperature specifications must be satisfied.
4. The case temperature should be measured by gluing a thermocouple to the top center of the component. This should be done with a 1mm bead of conductive epoxy, as defined by the JEDEC EIA/JESD51 standards. Care should be taken to ensure the thermocouple bead is touching the case.
5. Operating ambient temperature surrounding the package.

Table 12: Summary of Thermal Impedance

Die Size (mm^2)	Package	Number of Leads	Test Board	θ_{JA} (°C/W) 0m/s	θ_{JMA} (°C/W) 1m/s	θ_{JMA} (°C/W) 2m/s	θ_{JB} (°C/W)	θ_{JC} (°C/W)
94	TSOP	54	2-layer	62.6	48.4	44.2	19.2	6.7
			4-layer	39.2	32.3	30.6	19.3	

Figure 32: Example Temperature Test Point Location, 54-Pin TSOP: Top View

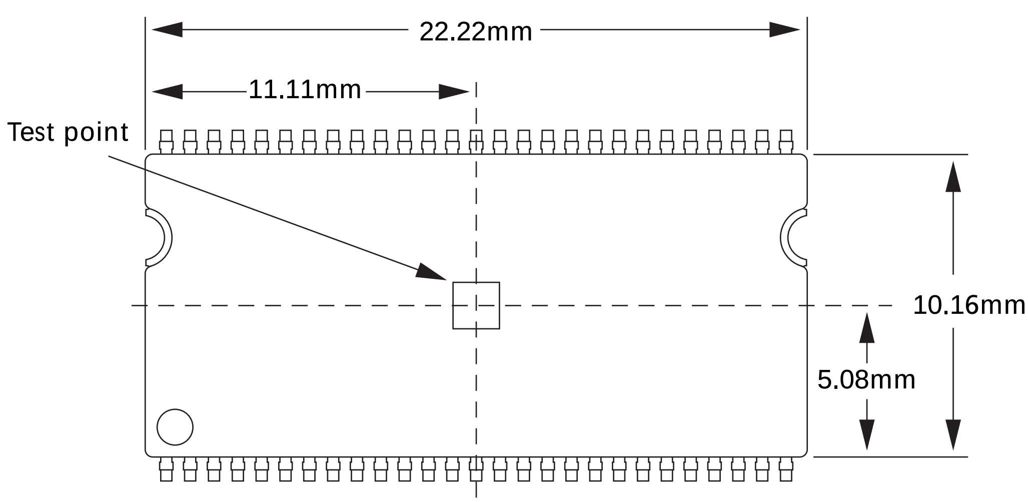


Table 13: DC Electrical Characteristics And Operating Conditions
Notes 1, 5, and 6 apply to entire table; notes appear on page 47; VDD, VDDQ = +3.3V ±0.3V

Parameter/Condition	Symbol	Min	Max	Units	Notes
Supply voltage	VDD, VDDQ	3	3.6	V	
Input high voltage: Logic 1; All inputs	VIH	2	VDD + 0.3	V	22
Input low voltage: Logic 0; All inputs	VIL	–0.3	0.8	V	22
Input leakage current: Any input 0V ≤ VIN ≤ VDD (All other pins not under test = 0V)	II	–5	5	µA	
Output leakage current: DQs are disabled; 0V ≤ VOUT ≤ VDDQ	IOZ	–5	5	µA	
Output levels: Output high voltage (IOUT = –4mA)	VOH	2.4	–	V	26
Output low voltage (IOUT = 4mA)	VOL	–	0.4	V	26

Table 14: IDD Specifications and Conditions
Notes 1, 5, 6, 11, and 13 apply to entire table; notes appear on page 47; VDD, VDDQ = +3.3V ±0.3V

Parameter/Condition		Symbol	Max		Units	Notes
			-7E	-75		
Operating current: Active mode; Burst = 2; READ or WRITE; ^tRC = ^tRC (MIN)		IDD1	120	110	mA	3, 18, 19, 29
Standby current: power-down mode; CKE = LOW; All banks idle		IDD2	3.5	3.5	mA	29
Standby current: Active mode; CS# = HIGH; CKE = HIGH; All banks active after ^tRCD met; No accesses in progress		IDD3	45	45	mA	3, 12, 19, 29
Operating current: Burst mode; Page burst; READ or WRITE; All banks active		IDD4	125	115	mA	3, 18, 19, 29
Auto refresh current: CS# = HIGH; CKE = HIGH	^tRFC = ^tRFC (MIN)	IDD5	255	255	mA	3, 18, 19, 29, 30
	^tRFC = 7.81µs	IDD6	6	6	mA	
Self refresh current: CKE ≤ 0.2V	Standard	IDD7	6	6	mA	•
	Low power (L)	IDD7	3	3	mA	

Table 15: Capacitance
Note 2 applies to entire table; notes appear on page 47

Parameter	Symbol	Min	Max	Units
Input capacitance: CLK	CI1	2.5	3.5	pF
Input capacitance: All other input-only pins	CI2	2.5	3.8	pF
Input/output capacitance: DQs	CIO	4.0	6.0	pF

Table 16: Electrical Characteristics and Recommended AC Operating Conditions
Notes 5, 6, 7, 8, 9, and 11 apply to entire table; notes appear on page 47

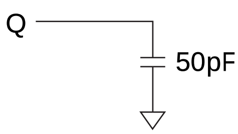
AC Characteristics			-7E		-75			
Parameter		**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Access time from CLK (positive edge)	CL = 3	$^tAC(3)$	–	5.4	–	5.4	ns	27
	CL = 2	$^tAC(2)$	–	5.4	–	6	ns	
Address hold time		^tAH	0.8	–	0.8	–	ns	
Address setup time		^tAS	1.5	–	1.5	–	ns	
CLK high-level width		^tCH	2.5	–	2.5	–	ns	
CLK low-level width		^tCL	2.5	–	2.5	–	ns	
Clock cycle time	CL = 3	$^tCK(3)$	7	–	7.5	–	ns	23
	CL = 2	$^tCK(2)$	7.5	–	10	–	ns	23
CKE hold time		^tCKH	0.8	–	0.8	–	ns	
CKE setup time		^tCKS	1.5	–	1.5	–	ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^tCMH	0.8	–	0.8	–	ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^tCMS	1.5	–	1.5	–	ns	
Data-in hold time		^tDH	0.8	–	0.8	–	ns	
Data-in setup time		^tDS	1.5	–	1.5	–	ns	
Data-out High-Z time	CL = 3	$^tHZ(3)$	–	5.4	–	5.4	ns	10
	CL = 2	$^tHZ(2)$	–	5.4	–	6	ns	10
Data-out Low-Z time		^tLZ	1	–	1	–	ns	
Data-out hold time (load)		^tOH	2.7	–	2.7	–	ns	
Data-out hold time (no load)		^tOH_N	1.8	–	1.8	–	ns	28
ACTIVE-to-PRECHARGE command		^tRAS	37	120,000	44	120,000	ns	
ACTIVE-to-ACTIVE command period		^tRC	60	–	66	–	ns	
ACTIVE-to-READ or WRITE delay		^tRCD	15	–	20	–	ns	
Refresh period (8,192 rows)		^tREF	–	64	–	64	ms	
AUTO REFRESH period		^tRFC	66	–	66	–	ns	
PRECHARGE command period		^tRP	15	–	20	–	ns	
ACTIVE bank *a* to ACTIVE bank *b* command		^tRRD	14	–	15	–	ns	
Transition time		^tT	0.3	1.2	0.3	1.2	ns	7
WRITE recovery time		^tWR	1 CLK + 7ns	–	1 CLK + 7.5ns	–	–	24
			14	–	15	–	ns	14, 25
Exit SELF REFRESH-to-ACTIVE command		^tXSR	67	–	75	–	ns	20

Table 17: AC Functional Characteristics
Notes 5, 6, 7, 8, 9, and 11 apply to entire table; notes appear below

Parameter		Symbol	-7E	-75	Units	Notes
READ/WRITE command-to-READ/WRITE command		^{t}CCD	1	1	^{t}CK	17
CKE to clock disable or power-down entry mode		^{t}CKED	1	1	^{t}CK	14
CKE to clock enable or power-down exit setup mode		^{t}PED	1	1	^{t}CK	14
DQM to input data delay		^{t}DQD	0	0	^{t}CK	17
DQM to data mask during WRITEs		^{t}DQM	0	0	^{t}CK	17
DQM to data High-Z during READs		^{t}DQZ	2	2	^{t}CK	17
WRITE command to input data delay		^{t}DWD	0	0	^{t}CK	17
Data-in to ACTIVE command		^{t}DAL	4	5	^{t}CK	15, 21
Data-in to PRECHARGE command		^{t}DPL	2	2	^{t}CK	16, 21
Last data-in to burst STOP command		^{t}BDL	1	1	^{t}CK	17
Last data-in to new READ/WRITE command		^{t}CDL	1	1	^{t}CK	17
Last data-in to PRECHARGE command		^{t}RDL	2	2	^{t}CK	16, 21
LOAD MODE REGISTER command to ACTIVE or REFRESH command		^{t}MRD	2	2	^{t}CK	26
Data-out to High-Z from PRECHARGE command	CL = 3	^{t}ROH(3)	3	3	^{t}CK	17
	CL = 2	^{t}ROH(2)	2	2	^{t}CK	17

Notes

1. All voltages referenced to VSS.
2. This parameter is sampled. VDD, VDDQ = +3.3V; f = 1 MHz, T_A = 25°C; pin under test biased at 1.4V.
3. IDD is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C for commercial; –40°C ≤ T_A ≤ 85°C for industrial) is ensured.
6. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (VDD and VDDQ must be powered up simultaneously. VSS and VSSQ must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
9. Outputs measured at 1.5V with equivalent load:

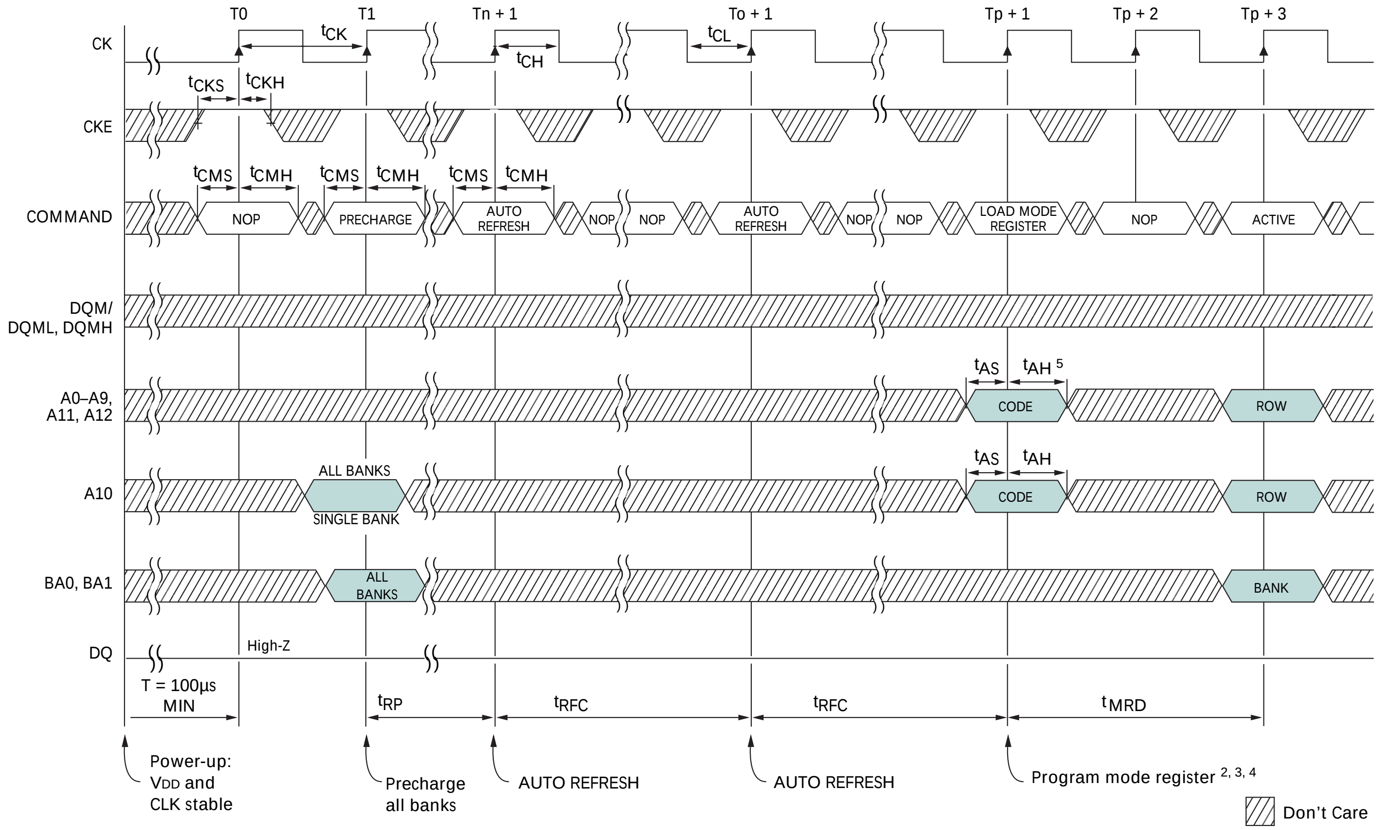


10. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to VOH or VOL. The last valid data element will meet ^{t}OH before going High-Z.
11. AC timing and IDD tests have VIL = 0V and VIH = 3V, with timing referenced to 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at VIL (MAX) and VIH (MIN) and no longer at the 1.5V crossover point. Refer to Micron technical note TN-48-09.
12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid VIH or VIL levels.
13. IDD specifications are tested after the device is properly initialized.
14. Timing actually specified by ^{t}CKS; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by ^{t}WR plus ^{t}RP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by ^{t}WR.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The IDD current will increase or decrease in a proportional amount by the amount the frequency is altered for the test condition.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on ^{t}CK = 7.5ns for -75 and -7E.

22. V_{IH} overshoot: V_{IH} (MAX) = V_{DDQ} + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one-third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = –2V for a pulse width ≤ 3ns for all inputs. V_{IH} overshoot for pin A12 is limited to V_{DDQ} + 1V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one-third of the cycle rate.
23. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including ^{t}WR, and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only. The precharge timing budget (^{t}RP) begins 7.5ns/7ns after the first clock delay, after the last WRITE is executed.
25. Precharge mode only.
26. JEDEC and PC100, PC133 specify three clocks.
27. ^{t}AC for -75/-7E at CL = 3 with no load is 4.6ns and is guaranteed by design.
28. Parameter guaranteed by design.
29. For -75, CL = 3, ^{t}CK = 7.5ns; for -7E, CL = 2, ^{t}CK = 7.5ns.
30. CKE is HIGH during refresh command period ^{t}RFC (MIN) else CKE is LOW. The I_{DD6} limit is actually a nominal value and does not result in a fail value.

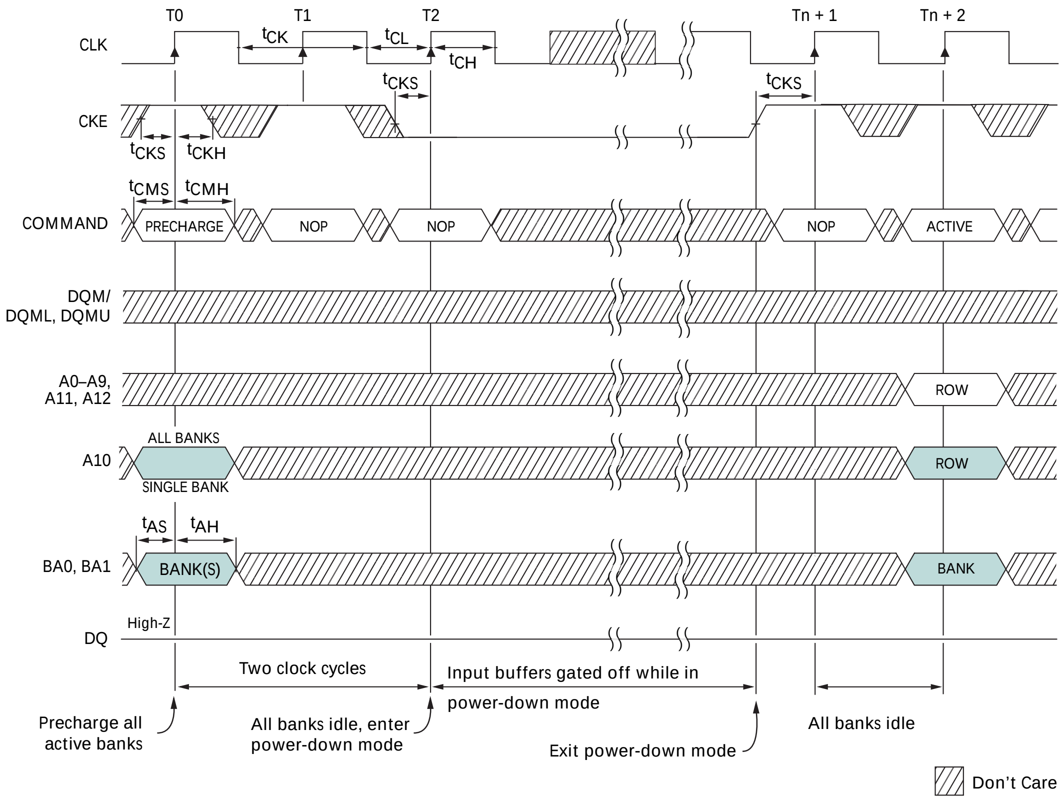
Timing Diagrams

Figure 33: Initialize and Load Mode Register



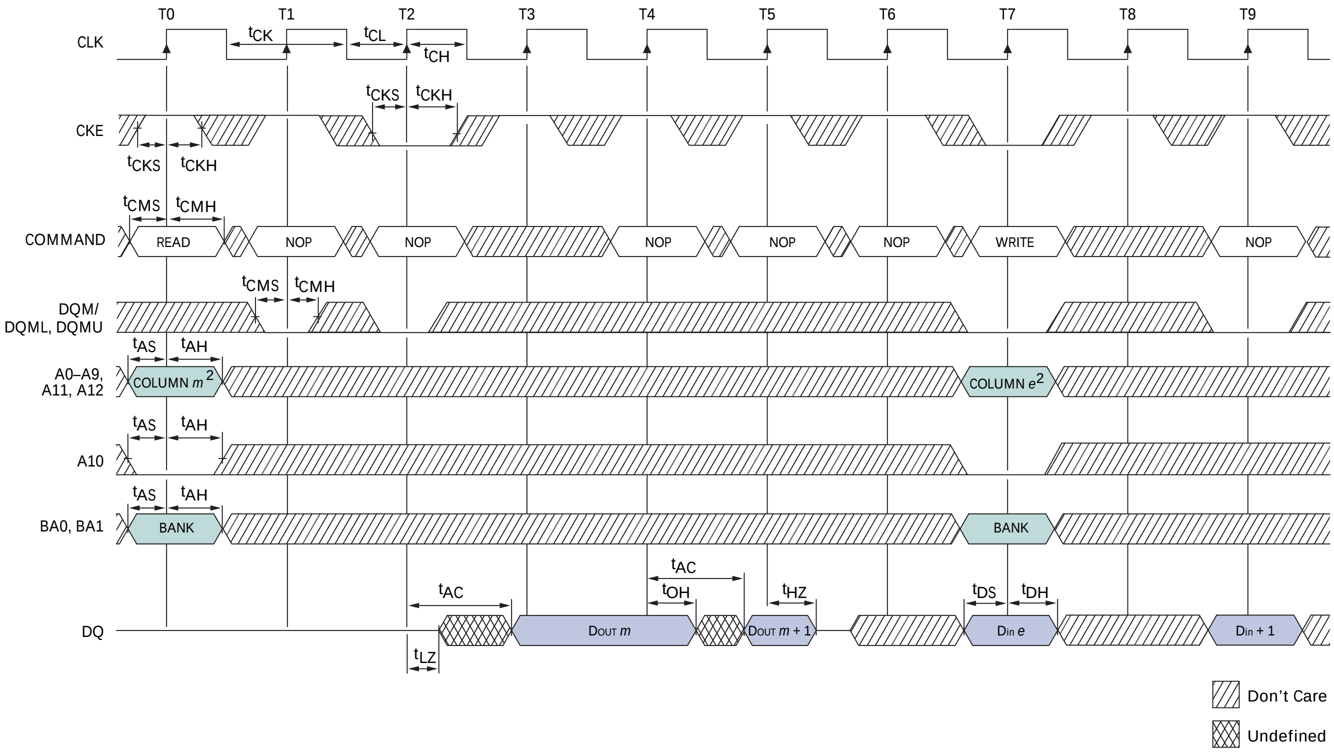
Notes:
1. If CS is HIGH at clock high time, all commands applied are NOP.
2. The mode register may be loaded prior to the AUTO REFRESH cycles if desired.
3. JEDEC and PC100 specify three clocks.
4. Outputs are guaranteed High-Z after command is issued.
5. A12 should be a LOW at Tp + 1.

Figure 34: Power-Down Mode



Note: Violating refresh requirements during power-down may result in a loss of data.

Figure 35: Clock Suspend Mode



Notes: 1. For this example, BL = 2, CL = 3, and auto precharge is disabled.
2. x16: A11 and A12 = "Don't Care"; x8: A12 = "Don't Care."

Figure 36: Auto-Refresh Mode

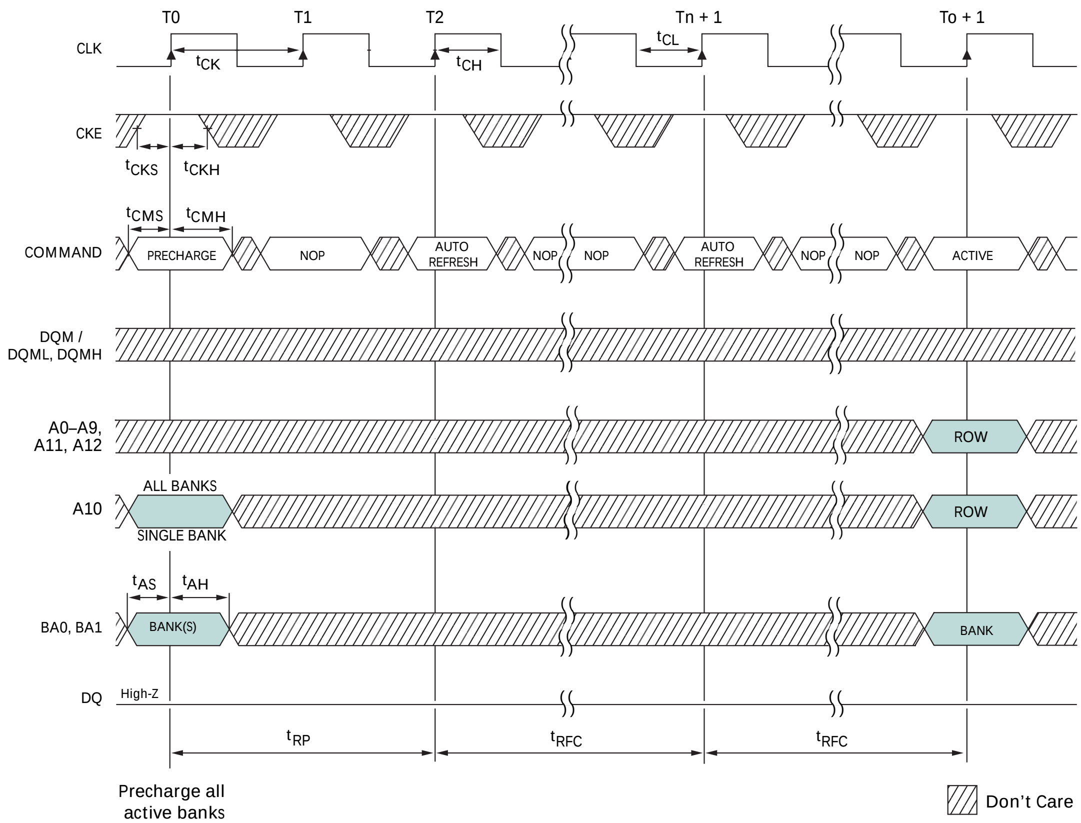
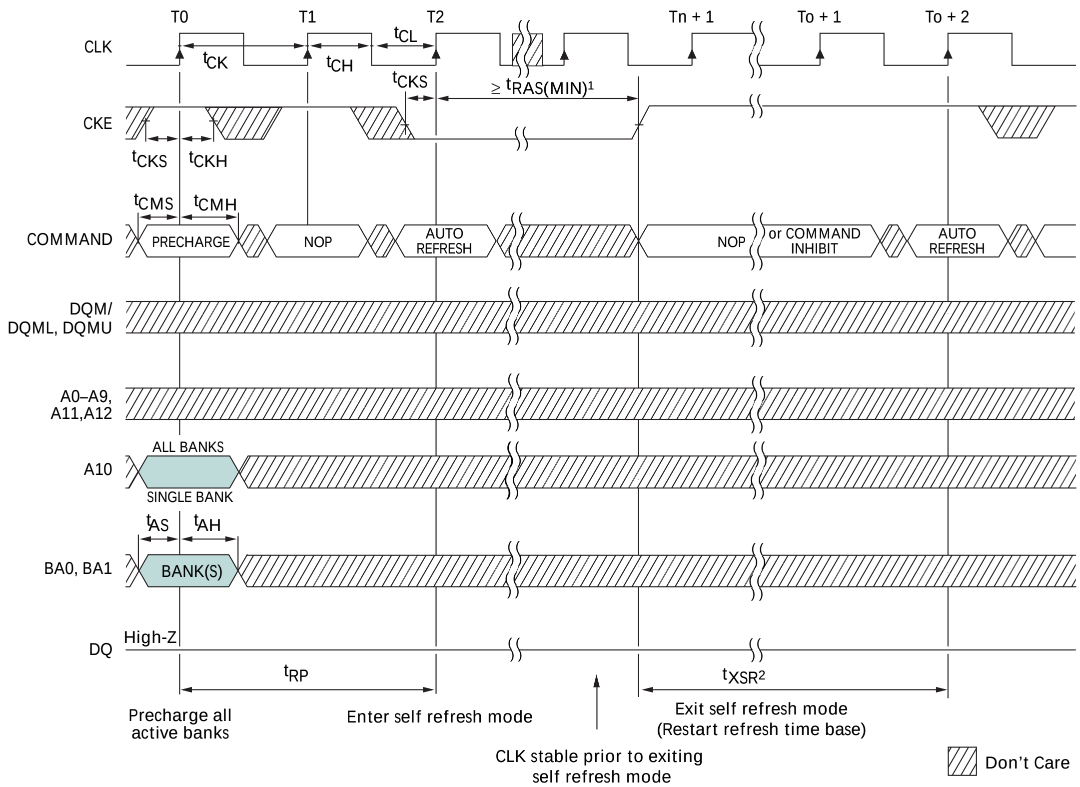
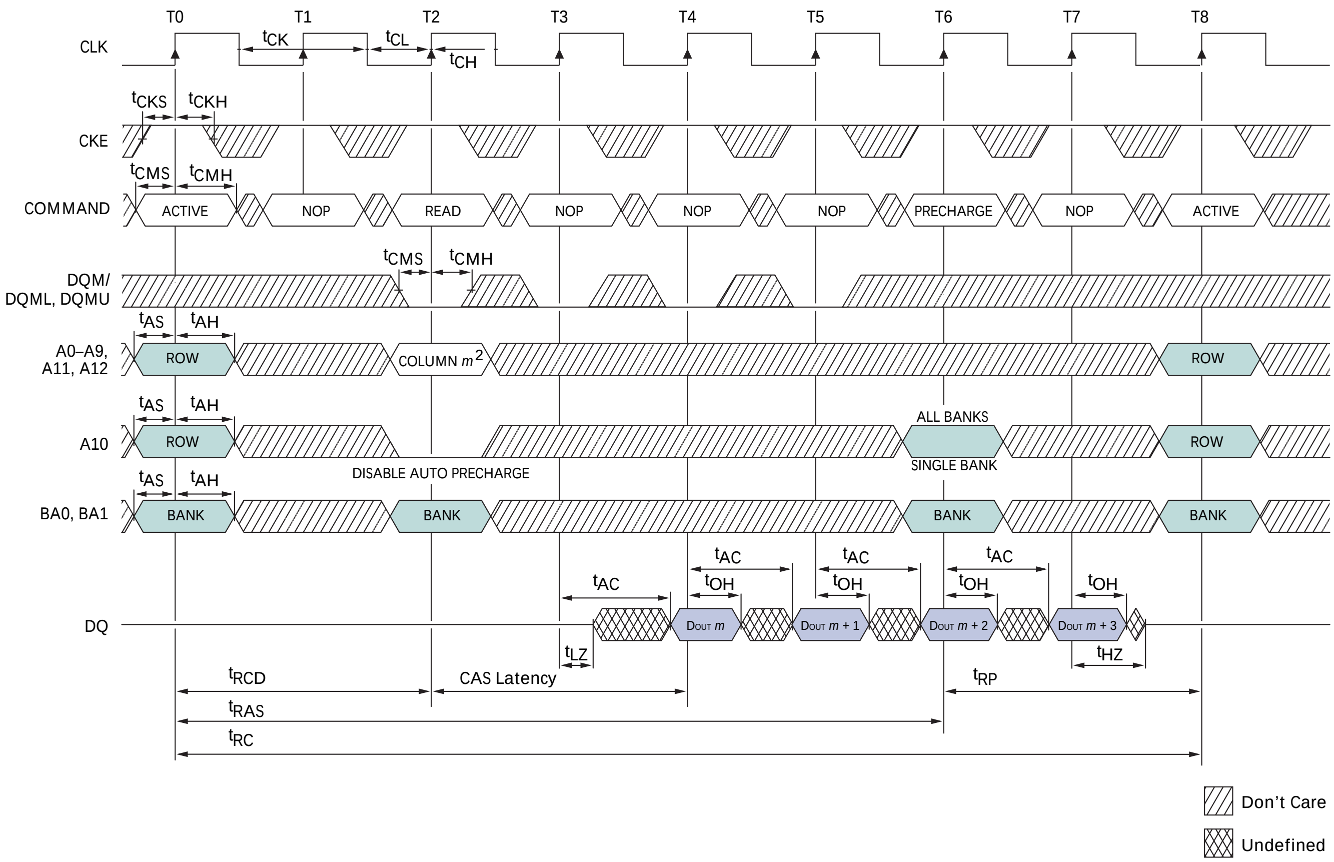


Figure 37: Self Refresh Mode



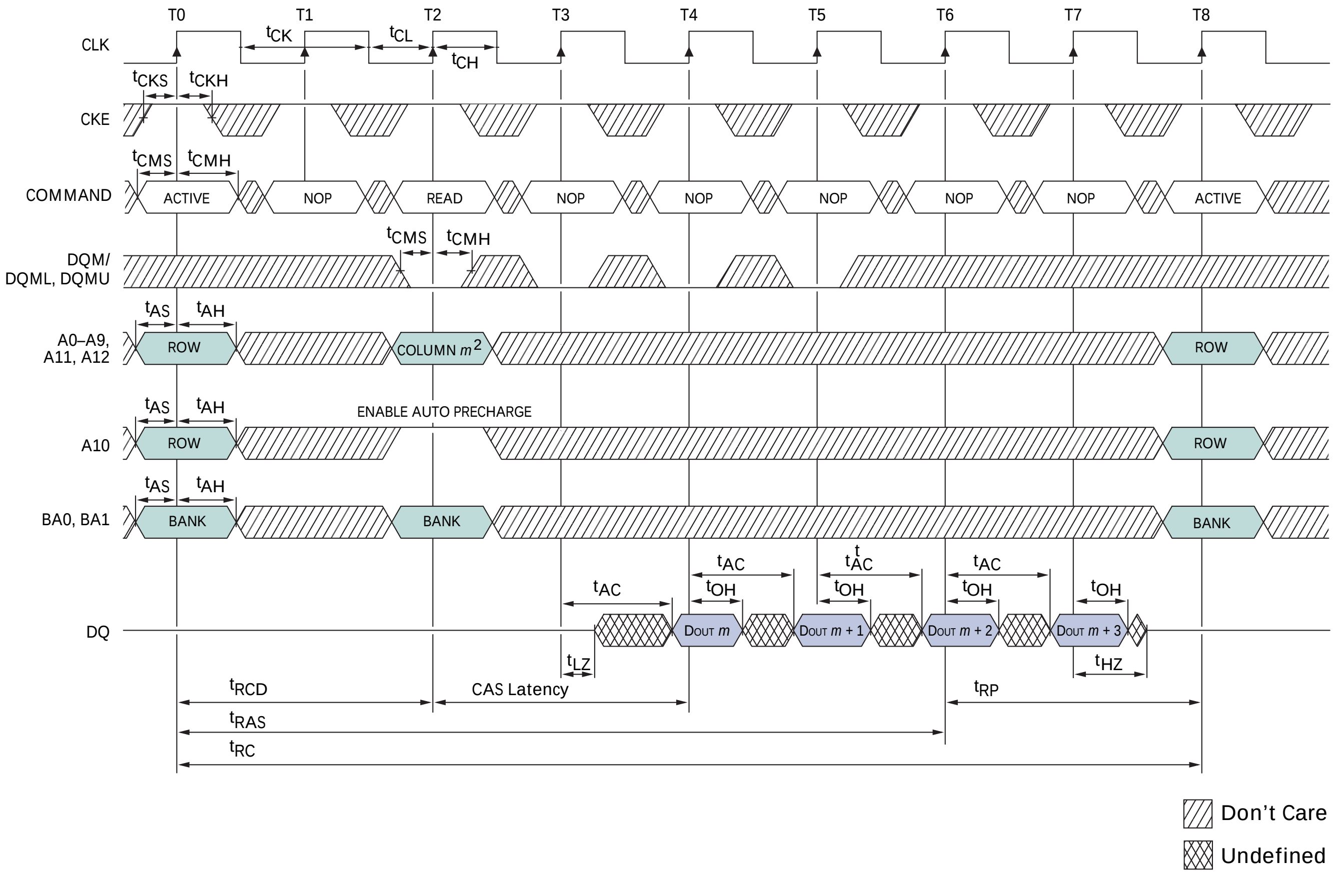
Notes: 1. No maximum time limit for self refresh; ^{t}RAS (MIN) applies to non-self refresh mode.
2. ^{t}XSR requires minimum of two clocks regardless of frequency or timing.

Figure 38: READ – Without Auto Precharge



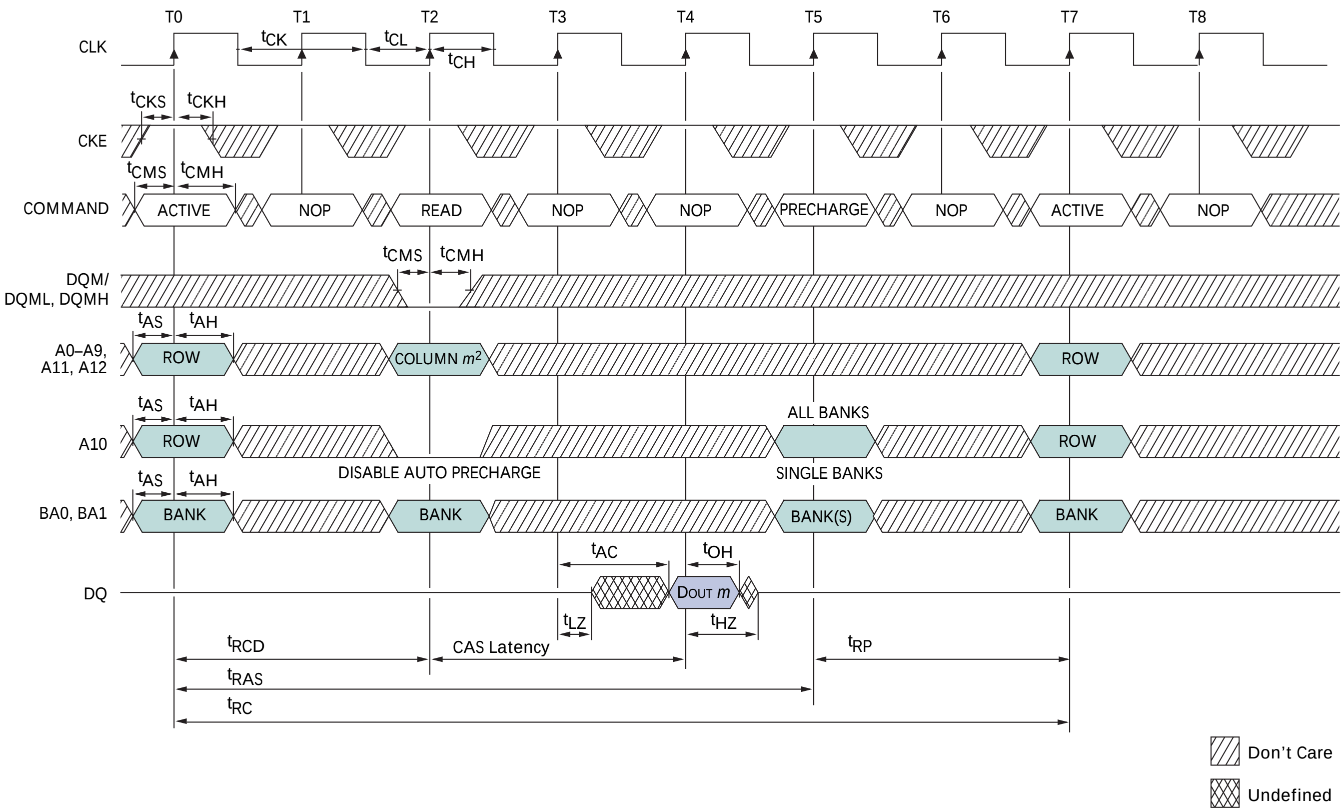
Notes:
1. For this example, BL = 4, CL = 2, and the READ burst is followed by a "manual" PRECHARGE.
2. x16: A11 and A12 = "Don't Care"; x8: A12 = "Don't Care."

Figure 39: READ – With Auto Precharge



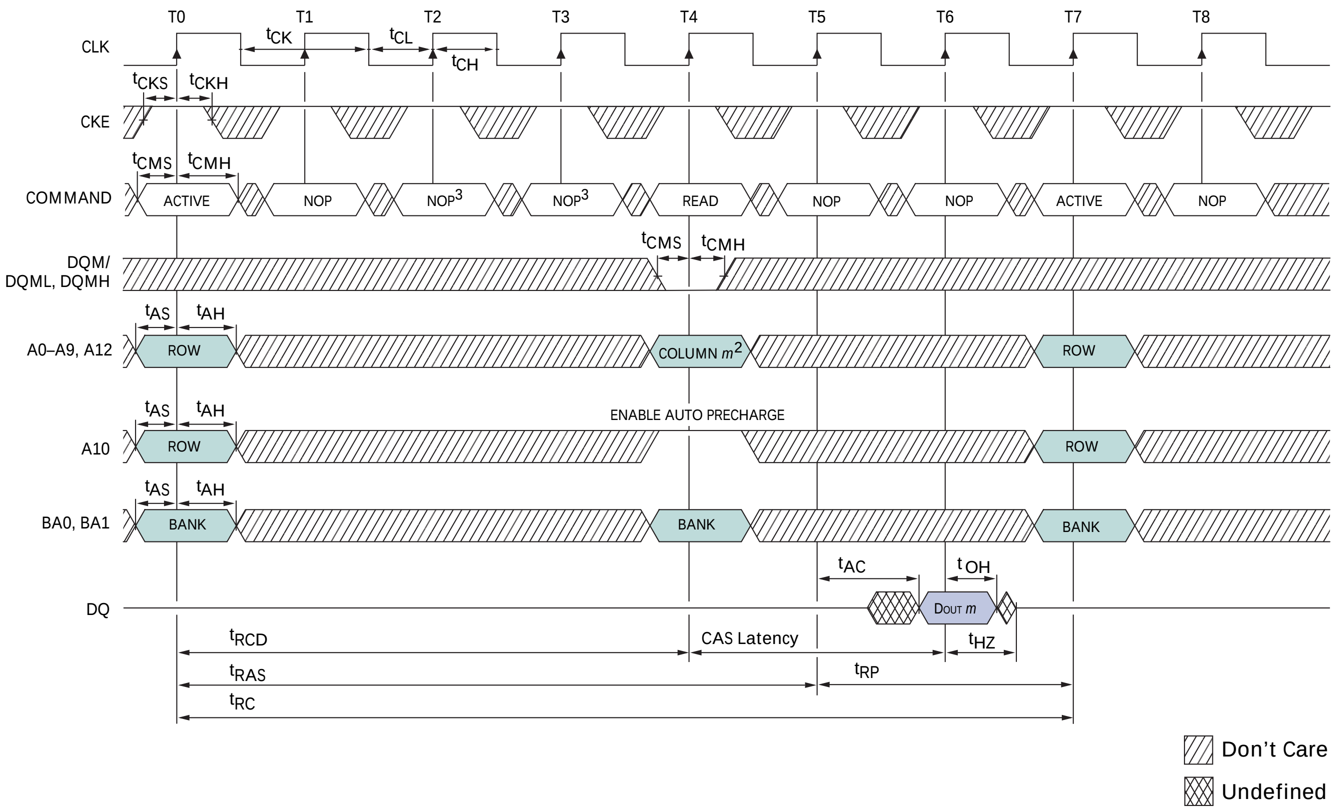
Notes: 1. For this example, BL = 4, and CL = 2.
2. x16: A11 and A12 = "Don't Care"; x8: A12 = "Don't Care."

Figure 40: Single READ – Without Auto Precharge



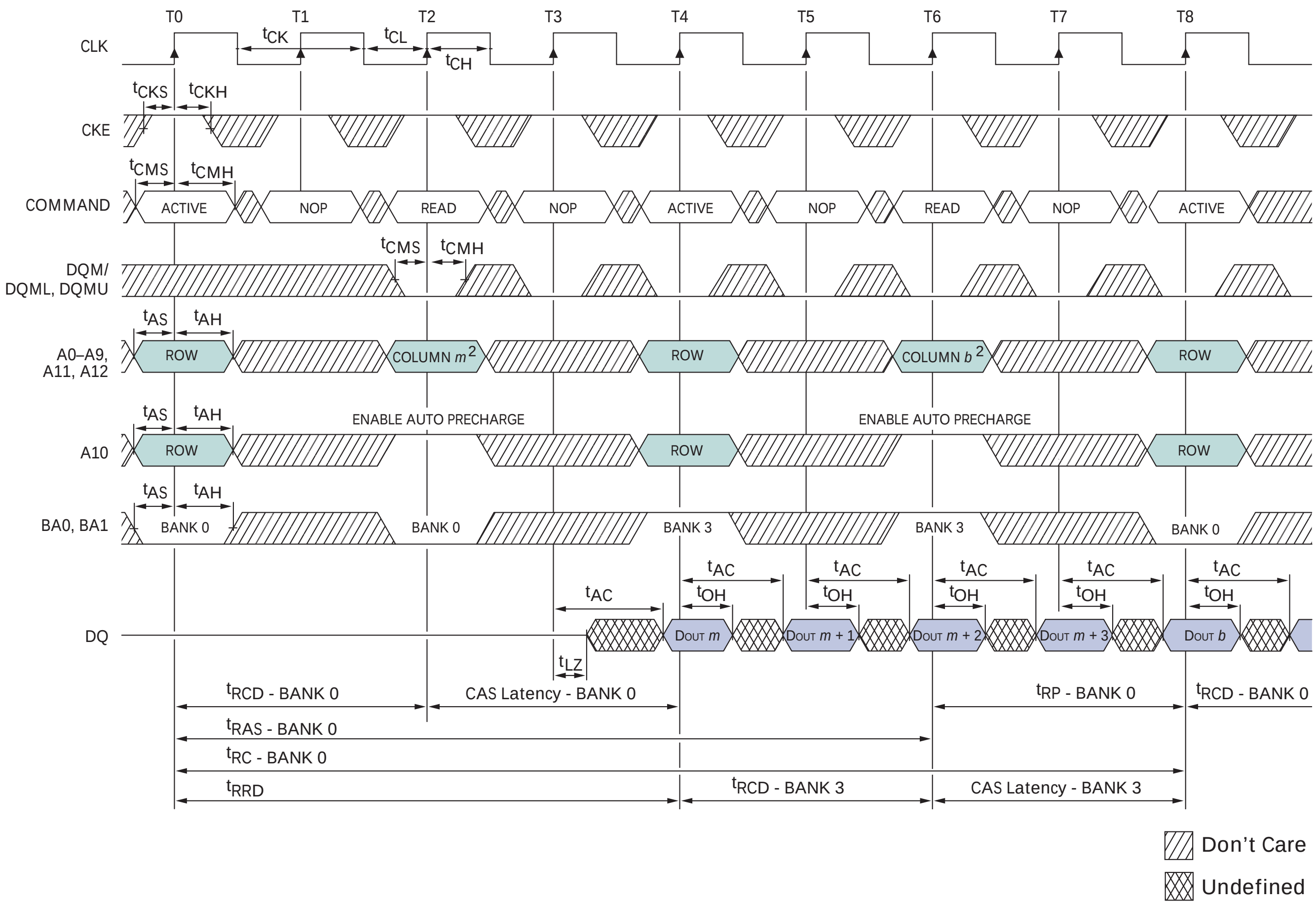
Notes: 1. For this example, BL = 1, CL = 2, and the READ burst is followed by a "manual" PRECHARGE.
2. x16: A11 and A12 = "Don't Care"; x8: A12 = "Don't Care."

Figure 41: Single READ – With Auto Precharge



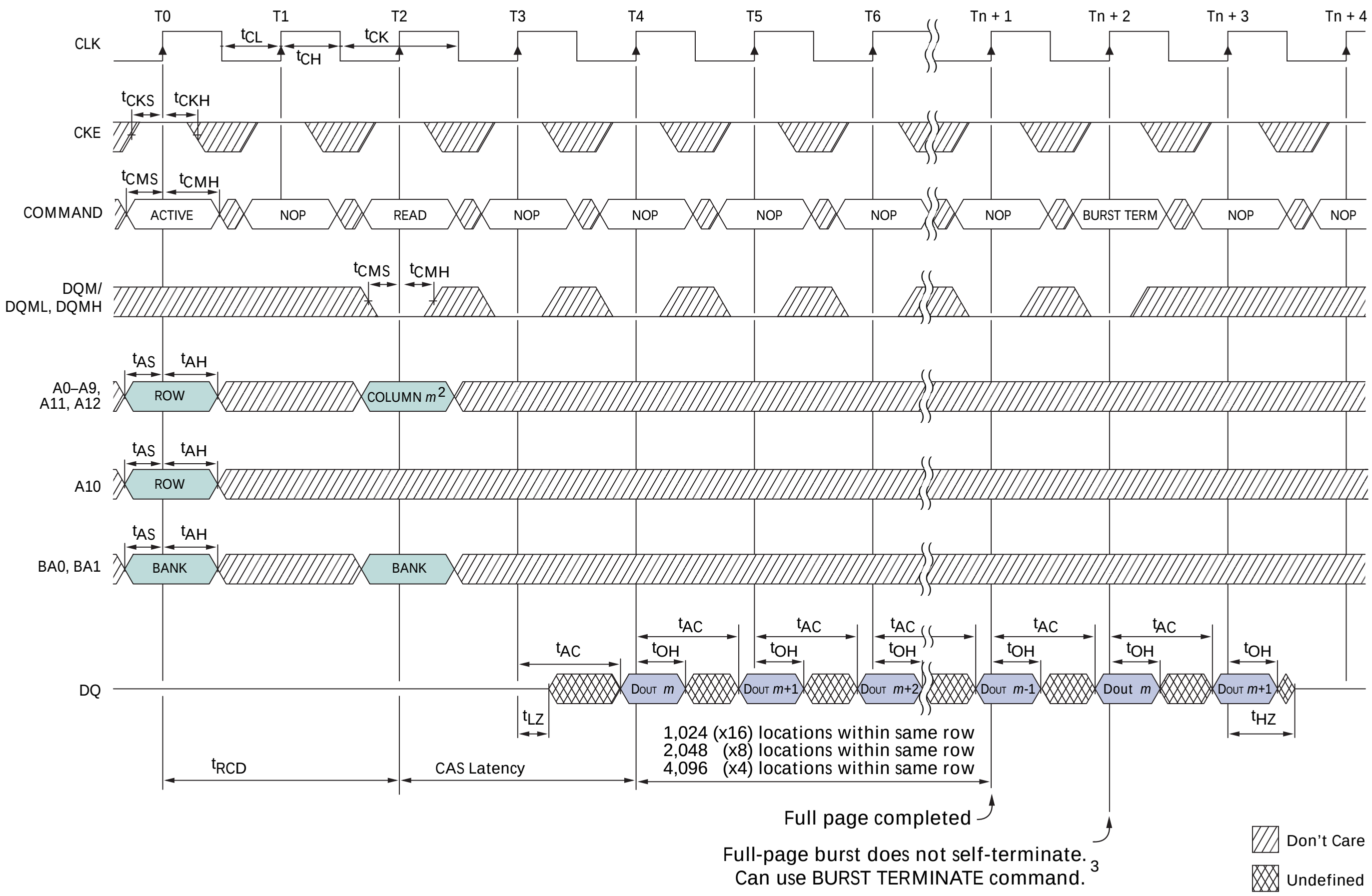
Notes:
1. For this example, BL = 1, and CL = 2.
2. x16: A11 and A12 = "Don't Care"; x8: A12 = "Don't Care."
3. READ command is not allowed else ^{t}RAS would be violated.

Figure 42: Alternating Bank Read Accesses



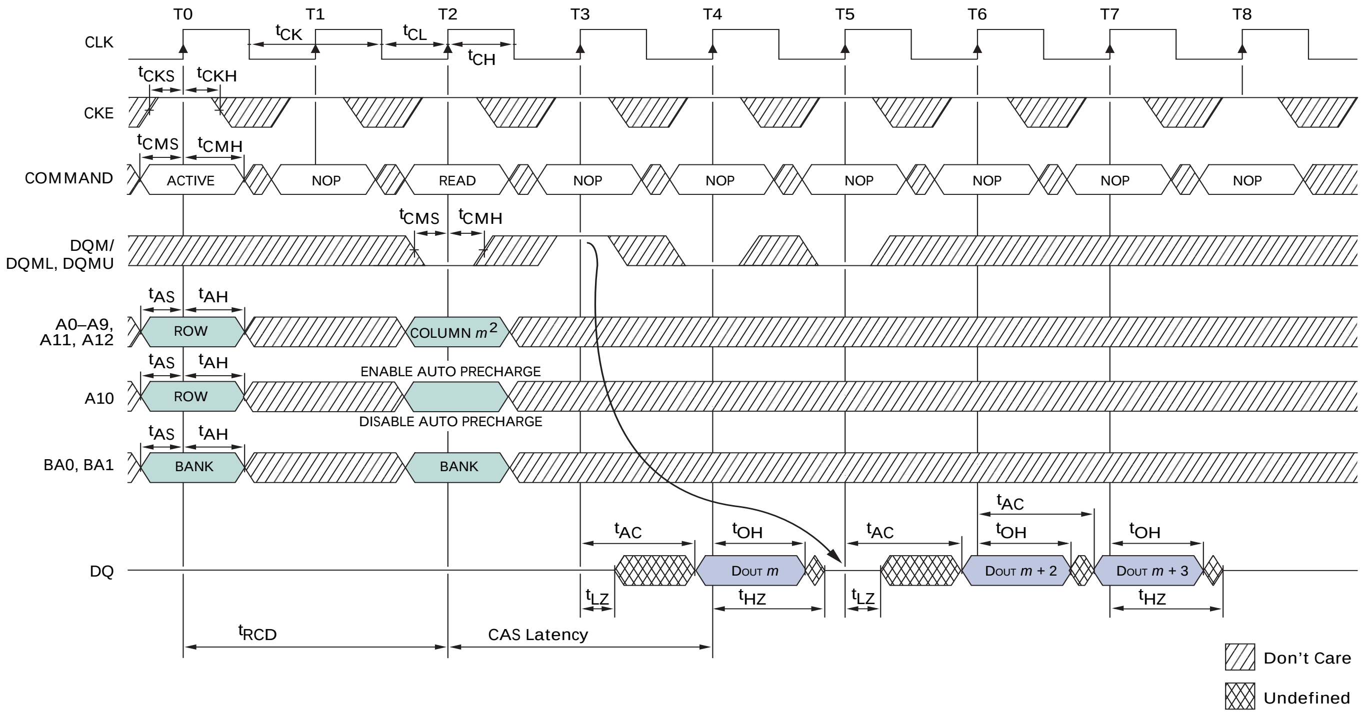
Notes:
1. For this example, BL = 4, and CL = 2.
2. x16: A11 and A12 = "Don't Care"; x8: A12 = "Don't Care."

Figure 43: READ – Full-Page Burst



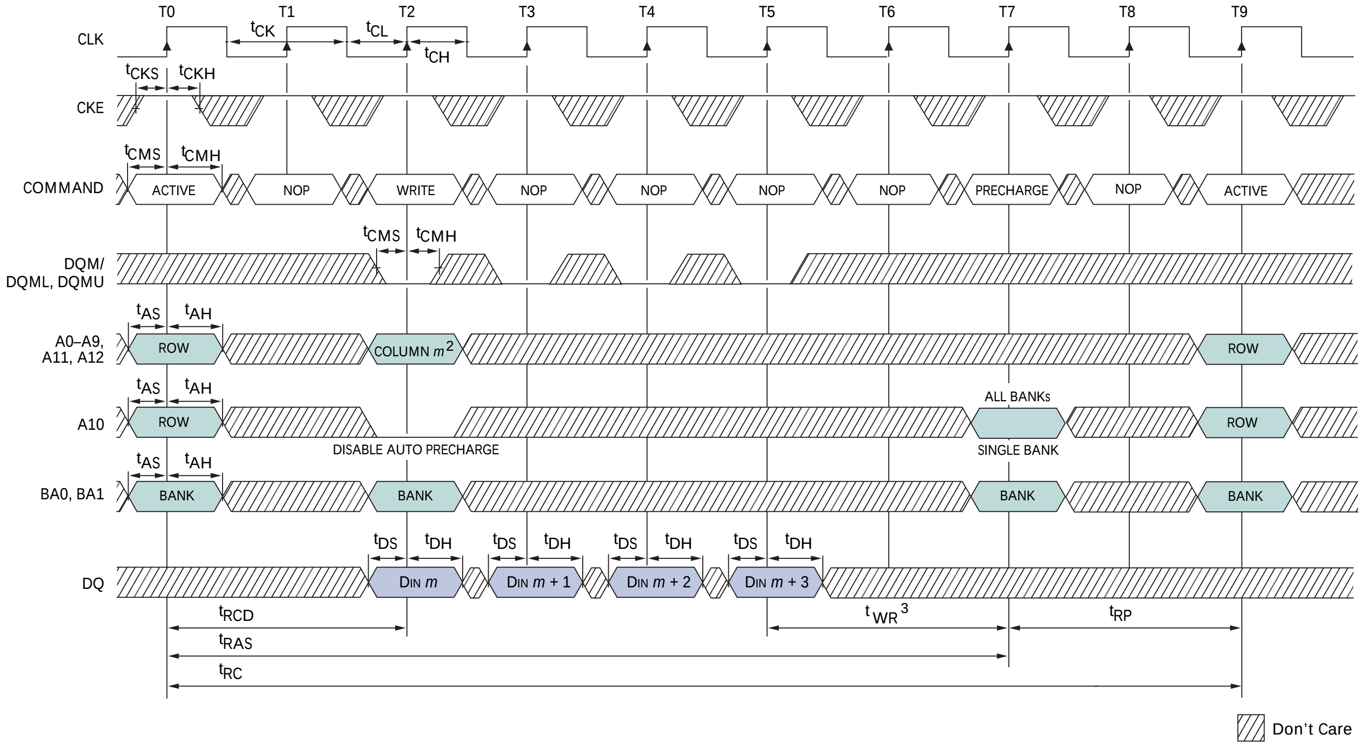
Notes:
1. For this example, CL = 2.
2. x16: A11 and A12 = "Don't Care"; x8: A12 = "Don't Care."
3. Page left open; no ^{t}RP.

Figure 44: READ DQM Operation



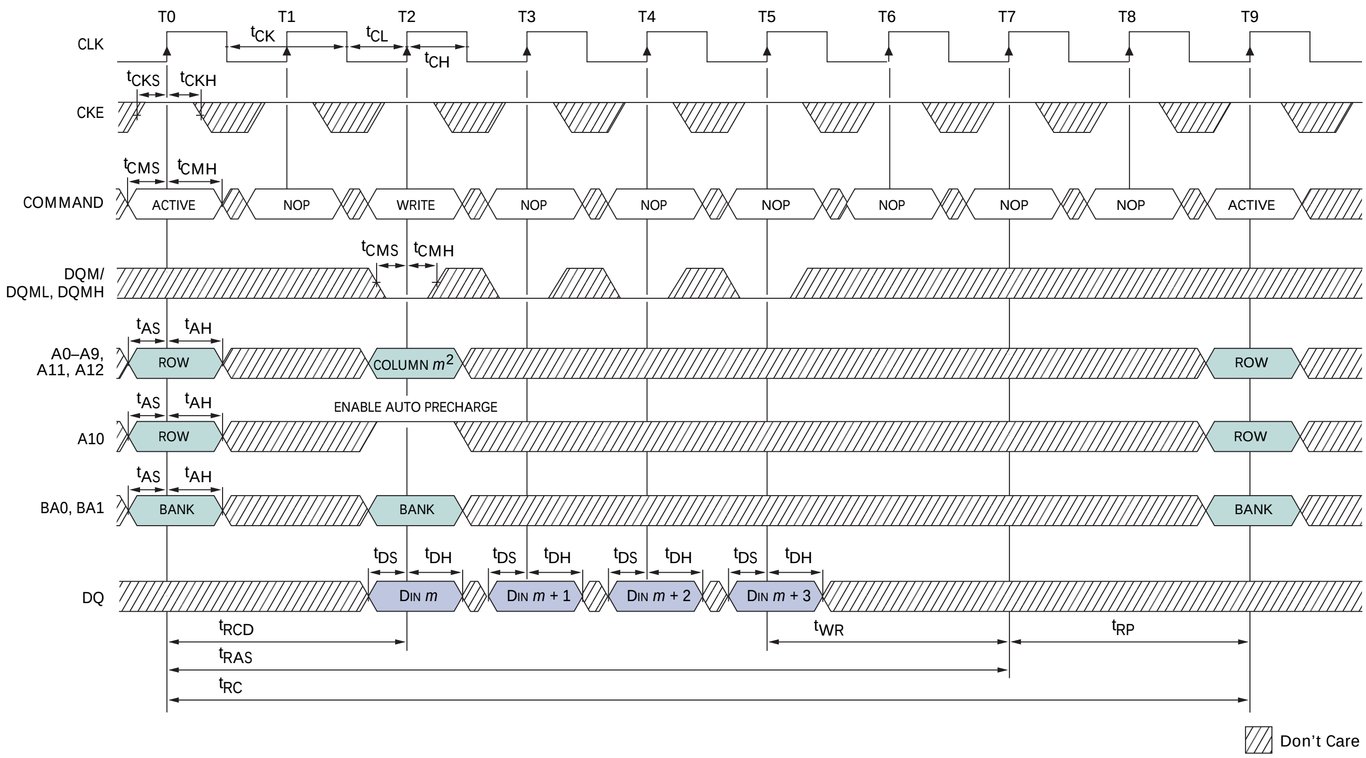
Notes:
1. For this example, BL = 4, and CL = 2.
2. x16: A11 and A12 = “Don’t Care”; x8: A12 = “Don’t Care.”

Figure 45: WRITE – Without Auto Precharge



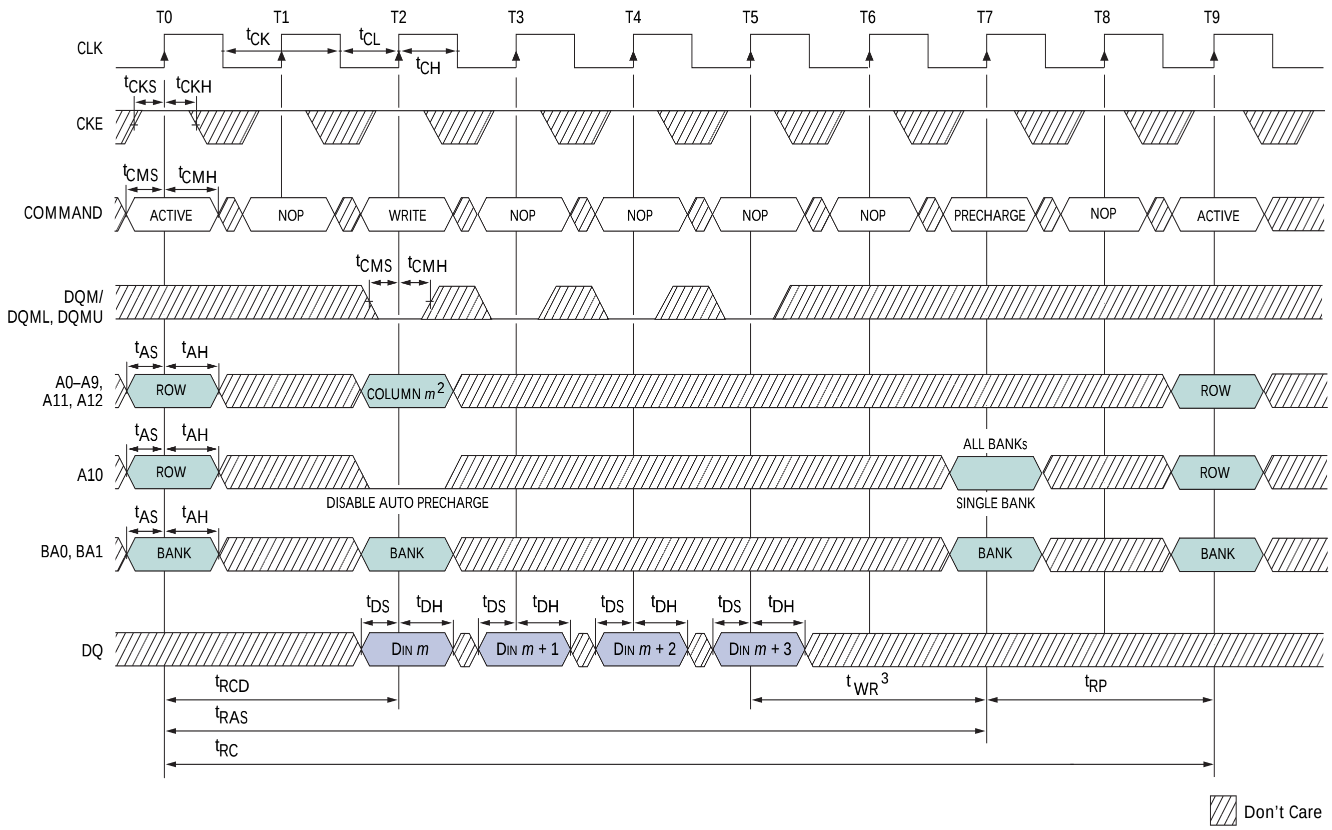
Notes:
1. For this example, BL = 4, and the WRITE burst is followed by a “manual” PRECHARGE.
2. 14ns to 15ns is required between <DIN *m*> and the PRECHARGE command, regardless of frequency.
3. x16: A11 and A12 = “Don’t Care”; x8: A12 = “Don’t Care.”

Figure 46: WRITE – With Auto Precharge



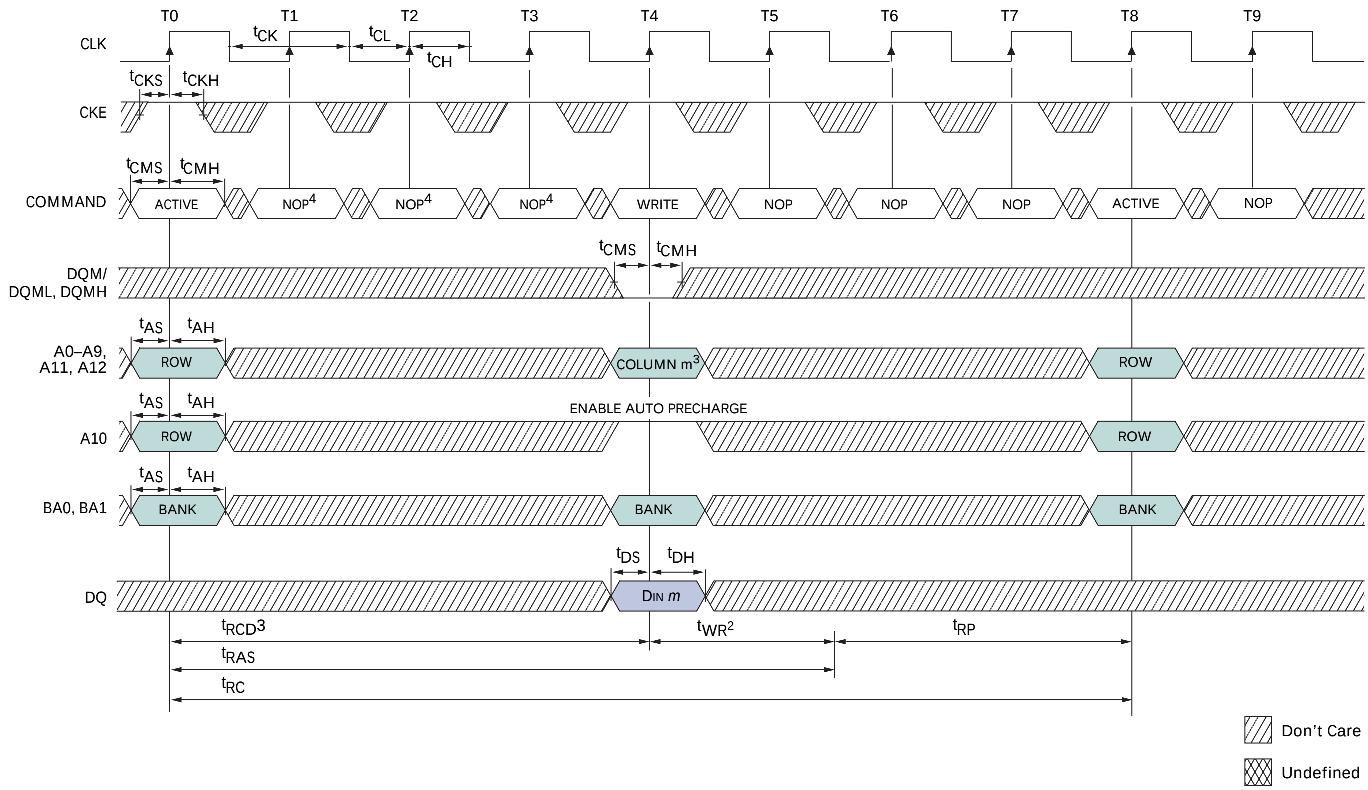
Notes: 1. For this example, BL = 4.
2. x16: A11 and A12 = "Don't Care"; x8: A12 = "Don't Care."

Figure 47: Single WRITE – Without Auto Precharge



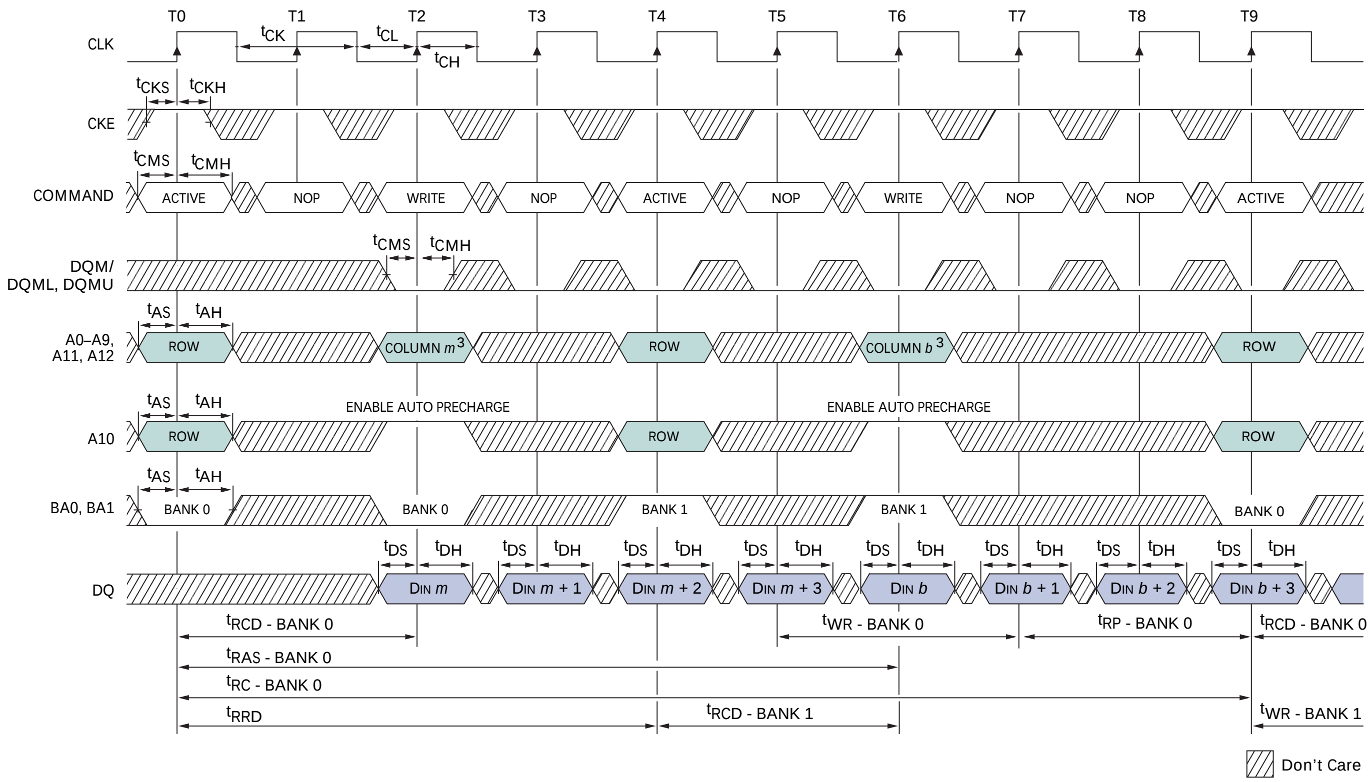
Notes:
1. For this example, BL = 1, and the WRITE burst is followed by a "manual" PRECHARGE.
2. 14ns to 15ns is required between <DIN *m*> and the PRECHARGE command, regardless of frequency.
3. x16: A11 and A12 = "Don't Care"; x8: A12 = "Don't Care."
4. PRECHARGE command not allowed else ^{t}RAS would be violated.

Figure 48: Single WRITE with Auto Precharge



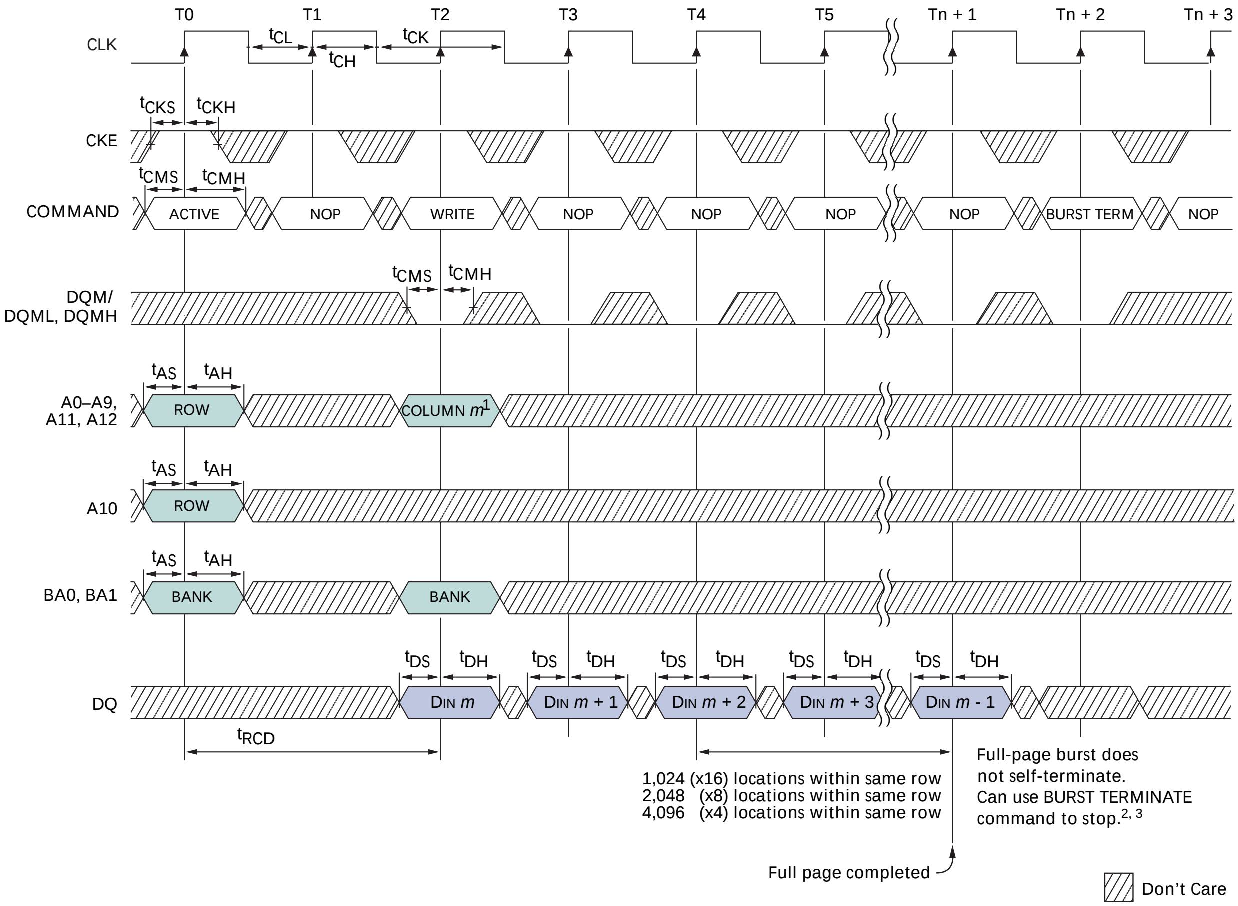
Notes:
1. For this example, BL = 1, and the WRITE burst is followed by a "manual" PRECHARGE.
2. 14ns to 15ns is required between <DIN *m*> and the PRECHARGE command, regardless of frequency.
3. x16: A11 and A12 = "Don't Care"; x8: A12 = "Don't Care."
4. WRITE command not allowed else ^{t}RAS would be violated.

Figure 49: Alternating Bank WRITE Accesses



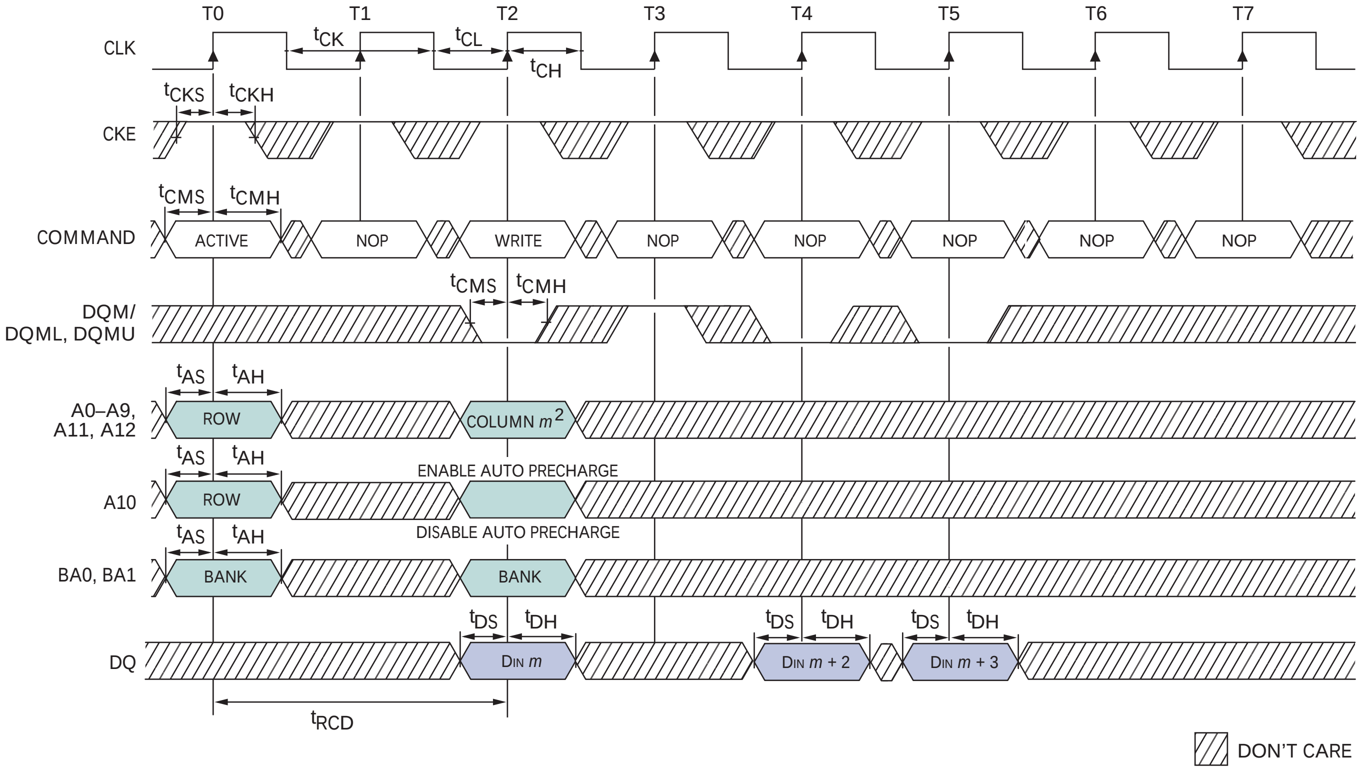
Notes:
1. For this example, BL = 4.
2. Requires one clock plus time (7ns to 7.5ns) with auto precharge or 14ns to 15ns with PRECHARGE.
3. x16: A11 and A12 = “Don’t Care”; x8: A12 = “Don’t Care.”

Figure 50: WRITE – Full-Page Burst



Notes:
1. x16: A11 and A12 = "Don't Care"; x8: A12 = "Don't Care."
2. ^{t}WR must be satisfied prior to PRECHARGE command.
3. Page left open; no ^{t}RP.

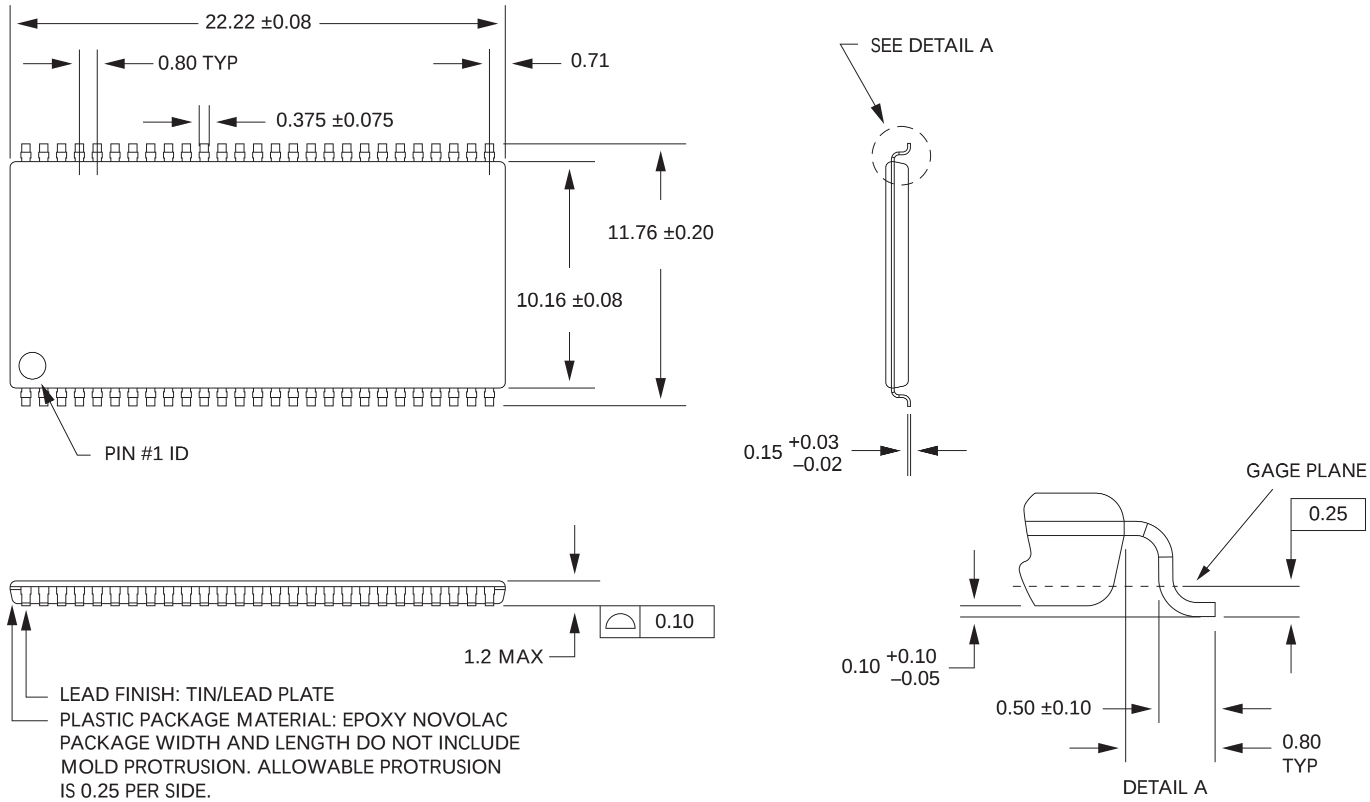
Figure 51: WRITE – DQM Operation



Notes:
1. For this example, BL = 4.
2. x16: A11 and A12 = "Don't Care;" x8: A12 = "Don't Care."

Package Dimensions

Figure 52: 54-Pin Plastic TSOP (400 mil)



Notes:
1. All dimensions in millimeters.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

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prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992

This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.